

**JITTER MEASUREMENT OF HIGH-SPEED DIGITAL  
SIGNALS USING LOW-COST SIGNAL ACQUISITION  
HARDWARE AND ASSOCIATED ALGORITHMS**

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Hyun Choi

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# JITTER MEASUREMENT OF HIGH-SPEED DIGITAL SIGNALS USING LOW-COST SIGNAL ACQUISITION HARDWARE AND ASSOCIATED ALGORITHMS

Approved by:

Abhijit Chatterjee, Advisor  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

David C. Keezer  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Saibal Mukhopadhyay  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Xiaoli Ma  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Hao Min Zhou  
School of Mathematics  
*Georgia Institute of Technology*

Date Approved: 29 June 2010

*To my beloved family*

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## SUMMARY

This dissertation proposes new methods for measuring jitter of high-speed digital signals. The proposed techniques are twofold. First, a low-speed jitter measurement environment is realized by using a jitter expansion sensor. This sensor uses a low-frequency reference signal as compared to high-frequency reference signals required in standard high-speed signal jitter measurement instruments. The jitter expansion sensor generates a low-speed signal at the output, which contains jitter content of the original high-speed digital signal. The low-speed sensor output signal can be easily acquired with a low-speed digitizer and then analyzed for jitter. The proposed low-speed jitter measurement environment using the jitter expansion sensor enhances the reliability of current jitter measurement approaches since low-speed signals used as a reference signal and a sensor output signal can be generated and applied to measurement systems with reduced additive noise.

The second approach is direct digitization without using a sensor, in which a high-speed digital signal with jitter is incoherently sub-sampled and then reconstructed in the discrete-time domain by using digital signal reconstruction algorithms. The core idea of this technique is to remove the hardware required in standard sampling-based jitter measurement instruments for time/phase synchronization by adopting incoherent sub-sampling as compared to coherent sub-sampling and to reduce the need for a high-speed digitizer by sub-sampling a periodic signal over its many realizations. In the proposed digitization technique, the signal reconstruction algorithms are used as a substitute for time/phase synchronization hardware.

When the reconstructed signal is analyzed for jitter in digital post-processing, a self-reference signal is extracted from the reconstructed signal by using wavelet

denoising methods. This digitally generated self-reference signal alleviates the need for external analog reference signals. The self-reference signal is used as a timing reference when timing dislocations of the reconstructed signal are measured in the discrete-time domain. Various types of jitter of the original high-speed reference signals can be estimated using the proposed jitter analysis algorithms.



# CHAPTER I

## INTRODUCTION

A leading trend of semiconductor manufacturing technology is to increase the integration density of integrated circuits (ICs) by shrinking the device feature size. The increased integration density gives IC systems more functionalities, computational power, and data handling capabilities. However, a functionality-rich system requires high-speed operation clocks and high-speed input/output (I/O) buses. Today, most high-speed I/Os are designed around 5 to 6 Gbps rates for copper-based channels. The bus speed of next generation devices will likely double or quadruple to 17 to 40 Gbps [33]. One consequence of this is that the multi-GHz clock and I/O speeds of digital processors and mixed-signal systems will provide significant challenges for jitter performance [23].

However, the cost of jitter measurement is significant [12, 59]. Current jitter analyzers require the use of high-speed sampling devices, accurate timing circuits, and high-performance storage systems and processors. For reliable jitter measurement, reference signals and other passive components need to be carefully designed and calibrated. The cost of jitter measurement increases with the rising speed of the signals to be measured.

To minimize the cost of jitter measurement, significant progress in measurement technology is mandatory. The desired jitter measurement techniques should be supported by reliable and low-cost measurement sub-systems to facilitate high-speed signal jitter measurement and analysis and to improve measurement accuracy while reducing its cost. In order to respond to the industry need for new jitter analyzers, this research focuses on the development of efficient and accurate jitter measurement

methods for high-speed digital signals.

As an introductory discussion, this chapter presents the relevant background of the research in this dissertation. Section 1.1 presents an overview of the current technology trend and emphasizes the need for jitter measurement. Section 1.2 describes jitter types and sources, followed by Section 1.3, which discusses research issues in jitter measurement of high-speed signals. Section 1.4 surveys and discusses previous approaches for jitter tests and measurement. After clarifying the limitations of the current methods, the last two sections introduce the proposed research in this dissertation.

## **1.1 Need for Jitter Measurement in High-Speed Digital Systems**

The quest for high-speed digital systems places significant demands on the performance of the underlying electronics and their data communication. As Moore's law predicts, more and more performance will be demanded of interchip data bandwidth. For error-free data communication, precise jitter performance and characterization are required from multi-Gbps serial data communication circuitry [18, 53]. It is well understood that the data communication bit error rate (BER) is directly related to the signal jitter value [26].

Non-ideal aspects of transmission lines such as crosstalk and losses have a negative impact on signal integrity and timing. These impacts dominate at multi-Gbps speed. Crosstalk noise has evolved as the key source of performance degradation and signal integrity problems in high-speed digital systems [1, 5, 7]. Crosstalk is the capacitive and inductive coupling of signals from one signal line to another. As the IC board speed and density increase, so does the problem of crosstalk. The impact of transmission line loss is also dominant in the era of high-speed signaling. Transmission line loss is frequency-dependent and causes distortion in the signal levels. These non-ideal aspects of transmission lines degrade the voltage and timing margins of the interchip

signaling link.

In the era of high-speed signaling, the timing requirement is tight [21,30,53]. The portions of timing budgets allocated to high-speed chip-to-chip interfaces are becoming smaller, making advanced timing measurement capabilities critically required. Major timing limitations on system level interconnections are the followings. First, increasing the bus signal speeds can make the signal rise times comparable to the propagation delays across the bus medium connecting IC's. If the electrical length of the bus medium is longer than the signal rise time, the transmission line effects of the medium is significant. This imposes impedance discontinuities and degrades the signal quality. Second, timing offset, or skew, creates another important limitation on system level interconnections. Skew results both from variation on the electrical characteristics of the bus ICs, and from the finite propagation speed of the signals through the bus conductors. In an ideal situation the bus clock events would occur at exactly the same time on every bus IC, causing data to be driven to or sampled from the bus simultaneously. Even when the clock distribution scheme is successful in minimizing skew, the bus clock still needs to be buffered internally on every bus IC. The unavoidable variation of the process and operating environment of the IC components introduces variations in the delay between the bus clock and the on-chip clocks. This variation degrades timing margins, and limits the maximum achievable transfer rate.

## **1.2 Jitter Types and Sources**

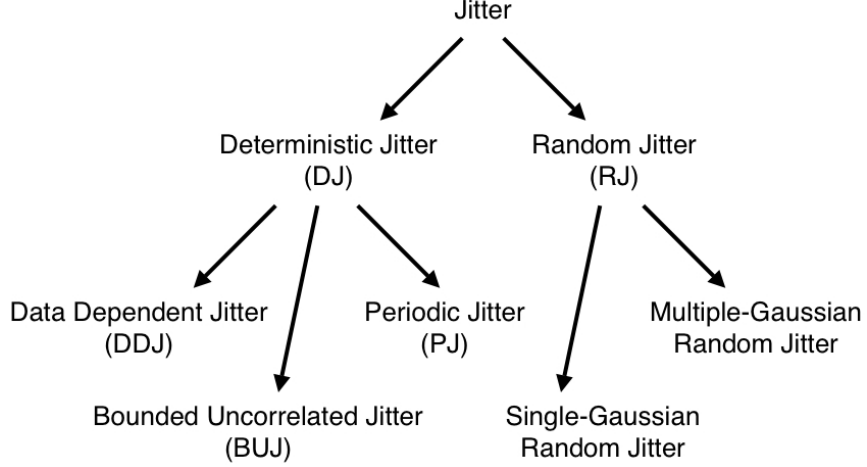
The International Telegraph and Telephone Consultative Committee (CCITT) has defined jitter as “short-term non-cumulative variation of the significant instants of a digital signal from their ideal positions in time.” In a digital signal, the significant instances are the transition points, and jitter is defined as the deviation of a timing event of a signal from its ideal occurrence in time.

Jitter can be classified into two major components: deterministic jitter and random jitter [43, 57]. Deterministic jitter is further classified into data dependent jitter (DDJ), periodic jitter (PJ), and bounded uncorrelated jitter (BUJ) [6]. Within deterministic jitter, DDJ is differentiated from the others based on whether or not the jitter correlates to the data pattern, hence it is also called correlated jitter. Prominent types of DDJ include duty-cycle distortion (DCD) and intersymbol interference (ISI). PJ, also called sinusoidal jitter, contains sinusoidal jitter components. Deterministic jitter that is not classified as DDJ or PJ is considered BUJ, which does not correlate to the data pattern and is not periodic, but it is bounded in amplitude. In comparison to deterministic jitter, random jitter exhibits random behavior and is unbounded in amplitude (random jitter is modeled using a Gaussian distribution). Random jitter is further classified into single-Gaussian random jitter or multiple-Gaussian random jitter.

Random jitter is caused by circuits' noise sources which are divided into two groups, namely, device noise and interference. Thermal, shot, and flicker noise are examples of the former, while power supply and substrate noise are in the latter group [22, 49]. These phenomena widely occur in semiconductor components, and therefore are encountered in oscillator topologies and phase-locked-loop designs [50]. On the other hand, deterministic jitter is caused by electromagnetic interference, crosstalk, signal reflection, driver slew rate, skin effects, and dielectric loss [24]. These are effects on a signal that result from the characteristics of its being a digital system in an analog environment.

### **1.3 Jitter Measurement Issues in High-Speed Signals**

The multi-GHz clock speeds of today's processors and mixed-signal systems pose significant challenges for jitter measurement. High-speed digitizers for such multi-GHz signals are not readily available and analysis of such signals is difficult due to



**Figure 1:** Sub-components of jitter.

the high cost of test equipment.

Several studies have been performed to investigate how the practical limitations of test resources can be overcome [10, 12, 27, 41, 42, 59, 60, 62, 63, 68]. Although many techniques have been developed to minimize dependency on wide-bandwidth test equipment, the test resolution of these methods is often degraded by measurement noise. To reduce the measurement noise caused by probe interfaces and interconnect, previous studies [27, 59, 63] have focused on how bit-error rate testers (BERT), phase noise meters, and oscilloscopes can be eliminated from the testing process through the adoption of built-in self-test (BIST) techniques. For instance, in some test methods, sensor circuits have been embedded on chips to analyze internal signals at critical circuit nodes. In other techniques, internal loopback is used to directly interface the transmitter output with the receiver input. Details of these techniques are discussed in Section 1.4. In the proposed approach, a low-speed jitter testing architecture is developed to alleviate the need for high-speed, wide-bandwidth testers and signal generators, the use of which have a significant impact on test cost.

## 1.4 Previous Research on Jitter Test and Measurement

There are many ways to categorize various jitter measurement methods. In this dissertation, the characteristics of the measurement circuit are used as the basis for categorizing. In some categories of jitter measurement, the term jitter is not explicitly used when parameters considered relevant to jitter, such as timing noise, phase noise, frequency instability and bit error rate (BER), are measured instead. It is well known that time-domain jitter is related to BER estimation and spectral characteristics of phase noise [17, 26].

### 1.4.1 Loopback BER Measurement

The first method for jitter measurement is the loopback test. To test digital communication systems, BER is commonly used as a measure of end-to-end system performance. It is measured by looping back the transmitter output to the receiver input. From the standpoint of jitter measurement, BER measurement is considered an alternative method. For integrated transceivers, the loopback test technique can reuse digital signal processor (DSP) and memory resources already available in the system, reducing test cost. However, BER testing has some limitations. First, it is not possible to test transmitters and receivers separately [12, 60]. If the performance of the transmitter is affected by process variations, a receiver on the same die may become equally unstable. Due to this reduced observability, some faults may be masked. Second, loopback requires the transmission of a large number of bits to estimate the BER. For instance, to test a 2.4-Gbps system with a BER of  $10^{-12}$ , it takes seven minutes on average to detect a single bit error [60]. Accordingly, measuring the BER of such a system requires several hours of testing time. This long test time makes loopback-based BER testing impractical in mass production.

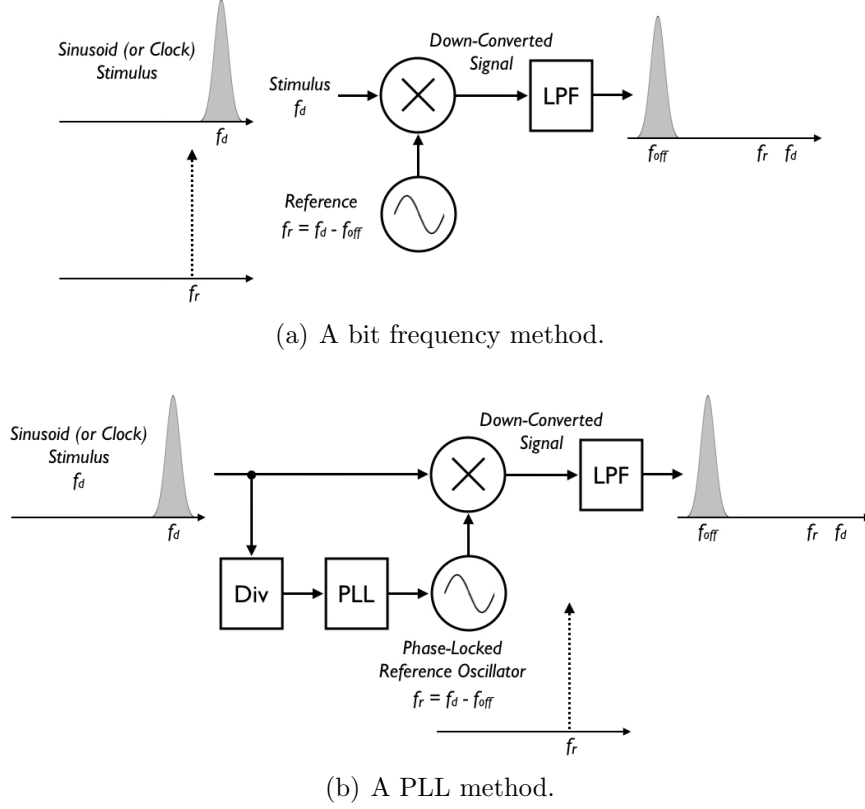
#### 1.4.2 Mixer-Based Phase Noise Measurement

The timing error of a digital clock signal can be measured by down-converting the signal using a mixer and analyzing the power spectrum of the resulting down-converted signal [56, 58, 67]. This requires a reference signal, whose frequency is close to that of the signal being down-converted. The mixer-based technique is further divided into the beat frequency method (or heterodyne measurement) and phase-locked loop (PLL) method (or homodyne measurement).

The beat frequency method is shown in Figure 2(a), in which the signal under test and the reference signal are fed into the two ports of a frequency mixer. The signal being tested is not necessarily synchronized with the reference signal in time and frequency, but the two signals are intended to have only a (small) frequency difference ( $f_{off}$  in Figure 2(a)). The beat frequency (the difference in frequency between the two input signals) is obtained as the output of a low pass filter which follows the mixer. This method uses the fact that jitter (or phase deviation from the ideal) is preserved by frequency translation. It is the beat frequency signal, and not the original signal, that is analyzed for jitter.

The PLL method is similar to the beat frequency method, but the reference signal needs to be synchronized with the signal under test in time and frequency. As shown in Figure 2(b), the reference signal is generated by a PLL-based frequency synthesizer which uses the divided version of the signal under test as a phase reference. Since the two input signals to the mixer are synchronized in frequency, the output signal of the mixer contains only a DC component. The phase fluctuations of the two input signals are integrated so that the voltage output of the mixer is proportional to the frequency fluctuations between the two input signals.

The down-converted signal (using a mixer) can be analyzed for jitter with various signal acquisition methods such as a point sampling, power spectrum sensing, or frequency counting. As compared to direct measurement, the down-converted signal is



**Figure 2:** Examples of mixer-based phase noise measurement technique.

at low-speed so that it can be acquired using low-speed signal acquisition equipments.

In the mixer-based methods, only the power spectrum of the fundamental tone is considered. This assumes that the phase noise of the harmonic terms is identical to that of the fundamental tone. (A digital clock signal contains multiple odd-order harmonics of the fundamental frequency). In addition, the noise of the high-speed reference signal (required to analyze a high-speed signal being tested) should be low since it contributes to the overall measurement noise. Thus, providing a low-noise, high-speed reference signal is a concern in the mixer-based techniques.

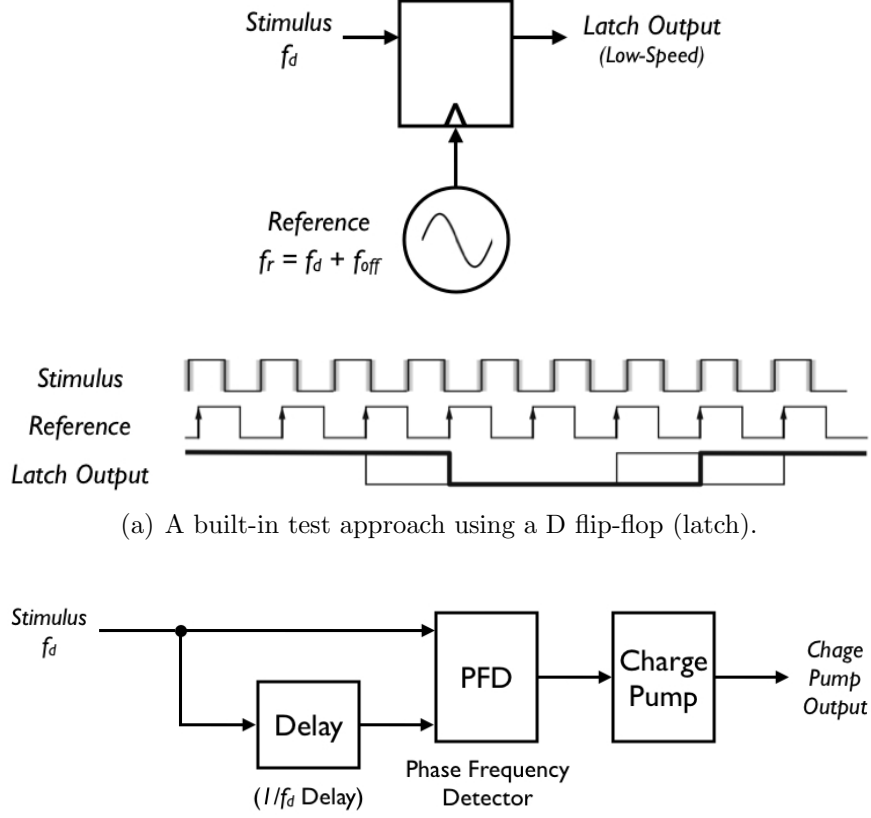
### 1.4.3 Built-In Jitter Measurement

Recently, various built-in test (BIT) techniques for jitter evaluation have been explored to alleviate the need for external measurement equipments and probing technologies [14]. When test circuits (or other equipment) are implemented on the same



die of the ICs to be tested, the test circuits can internally access the critical nodes (in signaling pathways) of the ICs. The use of on-chip BIT circuits raises concerns regarding additional die area and process variation effects on the test circuit itself [63]. These issues are addressed with BIT approach using a D flip-flop (latch) as proposed in [59]. As shown in Figure 3(a), the digital clock signal to be tested is fed to the latch while a reference clock signal is applied to the trigger port of the same latch. The reference clock signal contains a small frequency offset compared to the signal being tested. Due to the frequency offset, the two input signals to the latch drift away from each other in time so that the latch output signal is a low-speed (or beat-frequency) clock. In cases where the signal under test contains jitter, the latch output signal also shows timing deviations. In other words, the irregular toggling of the latch output signal corresponds to the jitter of the input signal being tested. This technique requires the use of a high-fidelity, high-speed clock reference signal. In addition, the output signal of the built-in latch needs to be very sensitive (in a deterministic sense) to small deviations of the transition edges of the input signal being tested.

Another BIT method utilizes a built-in delay circuit and phase frequency detector (PFD) [27]. This technique measures cycle-to-cycle jitter within a calibrated detectable range. As shown in Figure 3(b), the signal being tested (or stimulus) is split into two paths. One is fed directly into the PFD, and the other is fed to the delay line. The signal fed to the delay circuit is delayed by one cycle of the waveform. Instead of using an explicit reference signal, this technique uses the delayed signal as a reference signal. In the PFD, the signal being tested is compared to the one-cycle delayed replica of the same in terms of phase. (A charge pump translates the phase difference between the two input signals into a voltage value). The obtained voltage value (or fluctuation) at the charge pump output is correlated to the jitter value of the signal under test. In contrast to the latch-based BIT technique (described above), this method eliminates the need for a reference signal. Since it is difficult to



(a) A built-in test approach using a D flip-flop (latch).  
(b) A built-in test approach using a delay circuit and phase frequency detector.

**Figure 3:** Examples of built-in jitter test technique.

achieve a clean jitter-free on-chip reference clock, eliminating the use of the reference signal makes this test architecture suitable for on-chip jitter measurement. In [27], the implementation aspects of an accurate one-cycle delay are addressed in terms of programmable delay and calibration. However, these aspects need to be further addressed when process variation occurs.

## 1.5 Completed Research

The discussion in the previous section shows that the existing jitter measuring methods are not optimized in their applicability to high-speed signal jitter measurements. Therefore, this dissertation research aims to propose and verify a new methodology for enhancing the applicability of jitter measurement systems by designing a simplified

signal acquisition architecture.

The following work has been completed in this dissertation.

- **Jitter sensor design for enhanced jitter measurements in low-speed test environments:** A time-domain jitter expansion technique is introduced to enable high-fidelity jitter testing of high-speed signals. A special circuit called a jitter sensor is used for jitter extraction. This sensor produces a low-speed output signal with expanded jitter, in which the output signal jitter is a multiple of the input jitter along the time scale. This jitter expansion makes a low-speed test environment possible, which alleviates the need for wide-bandwidth testers. A narrow-bandwidth, low-speed digitizer is used to acquire the sensor output signal. The proposed approach enables high-resolution jitter testing of high-speed signals at low cost.
- **Simplified signal acquisition architecture design using incoherent sub-sampling and back-end signal reconstruction algorithms:** A high-speed periodic signal acquisition technique using incoherent sub-sampling and back-end signal reconstruction algorithms is presented. The signal reconstruction algorithms employ a frequency domain analysis for frequency estimation and suppression of jitter-induced sampling noise. If the sampling rate of a digitizer is switched, the analog frequency value of the sampled signal can be recovered. The proposed signal reconstruction uses incoherent sub-sampling to reduce hardware complexity. The results of simulation and hardware experiments indicate that the proposed signal reconstruction algorithms are able to reconstruct multi-tone high-speed periodic signals in the discrete time domain. The new signal acquisition technique simplifies signal acquisition hardware for testing and characterization of high-speed analog and digital signals.

- **Jitter characterization of incoherently sub-sampled high-speed digital signals:** A jitter characterization approach for incoherently sub-sampled high-speed digital signals using back-end signal processing algorithms is presented. Signal sub-sampling is used to increase the effective sampling rate of the digitizer used for data acquisition, while incoherent sampling is utilized to simplify the data acquisition hardware. Algorithms for signal clock recovery (CR) and waveform reconstruction from the acquired data are developed in this research. The algorithms utilize peak identification of the sampled signal spectrum and the sparsity of the reconstructed waveform in the frequency domain as decision criteria for accurate signal reconstruction. The jitter value of such a reconstructed waveform is quantified with the use of a wavelet based denoising method to generate a self-reference signal against which zero-crossing times are compared to generate jitter statistics. In addition, the data dependent jitter components can be differentiated from the original jitter by analyzing zero-crossing discrepancies of the self-reference signal.

## 1.6 Dissertation Outline

The rest of this dissertation consists of the following chapters. Chapter 2 proposes a jitter expansion sensor which enables a low-speed test environment. It then presents details of time-domain jitter expansion using a low-speed reference signal and the following low-speed digitization method. Chapter 3 discusses a new direct digitization method, which simplifies the signal acquisition architecture of non-realtime sampling systems. Chapter 4.1 proposes a software CR method. This software CR technique (as compared to hardware CR) is essential for the simplified signal acquisition architecture described in Chapter 3. Chapter 4.2 discusses a jitter quantization method in the discrete-time domain. Also presented are details of jitter decomposition and quantization as well as self-reference signal generation using a wavelet-based denoising

method. Chapter 5 concludes this dissertation and proposes future work.

## CHAPTER II

### JITTER TESTING WITH LOW-SPEED TESTERS USING A JITTER EXPANSION SENSOR

#### 2.1 Jitter Modeling

A digital signal with jitter is modeled as a series of rising and falling exponential functions with random duty cycle [44, 52, 66]. To address finite slew rate due to bandwidth limitations of communication channels and transceivers, a simple RC interconnect model is utilized. The modeled digital signal with jitter  $d(t)$  is shown in Equations 1–9.

$$d(t) = A_d \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(t) \cdot e_i(t) \quad (1)$$

where  $A_d$  is the signal amplitude;  $i$  represents the bit index;  $\alpha_i$  defines the bit switching of the  $i$ -th bit:

$$\{\alpha_0, \dots, \alpha_n\} \subset \{-1, 0, +1\}, \quad (2)$$

$$\alpha_k \cdot \alpha_{k+1} \neq 1 \quad (3)$$

where the  $\{-1, 0, +1\}$  in Equation 2 represents the {falling, no switching, rising} of the bit;  $A_i$  defines the time interval with jitter:

$$A_i = [t_i, +\infty), \quad (4)$$

$$t_i = i \cdot \frac{T_d}{2} + \Delta t_i \quad (5)$$

with  $\Delta t_i$  denoting the timing error and  $T_d$  denoting the ideal bit width;  $1_{A_i}$  is the indicator function of  $A_i$ :

$$1_{A_i}(t) = \begin{cases} 1 & t \in A_i \\ 0 & \text{otherwise} \end{cases}; \quad (6)$$

and  $e_i(t)$  is the exponential function:

$$e_i(t) = 1 - e^{-\frac{t-t_i}{\tau_d}} \quad (7)$$

with  $\tau_d$  denoting the time constant. To derive  $\Delta t_i$  using computer simulation, the phase noise model of an LC oscillator in [22] is used under the assumption that the phase noise of the LC oscillator as a time-base signal generator is directly related to the timing error of  $d(t)$ . According to this phase noise model, the output excess phase  $\Delta\phi_d(t)$  of the oscillator is calculated using the superposition integral:

$$\Delta\phi_d(t) = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_0\tau) i(\tau) d\tau \quad (8)$$

where  $q_{max}$  is the maximum charge displacement across the capacitor,  $\Gamma(\omega_0\tau)$  denotes the (periodic) impulse sensitivity function, and  $i(\tau)$  represents the input noise current injected into the node of interest.  $i(\tau)$  is random stationary, and  $\Delta\phi_d(t)$  is an accumulated value of  $\Gamma(\omega_0\tau)i(\tau)$  (random cyclostationary increments) up to  $t$ . To relate  $\Delta\phi_d(t)$  to  $t_i$  which is used in Equation 5, the zero-crossing of the modeled LC oscillator output signal  $s(t)$  is represented using  $t_i$  and  $\Delta\phi_d(t_i)$ :

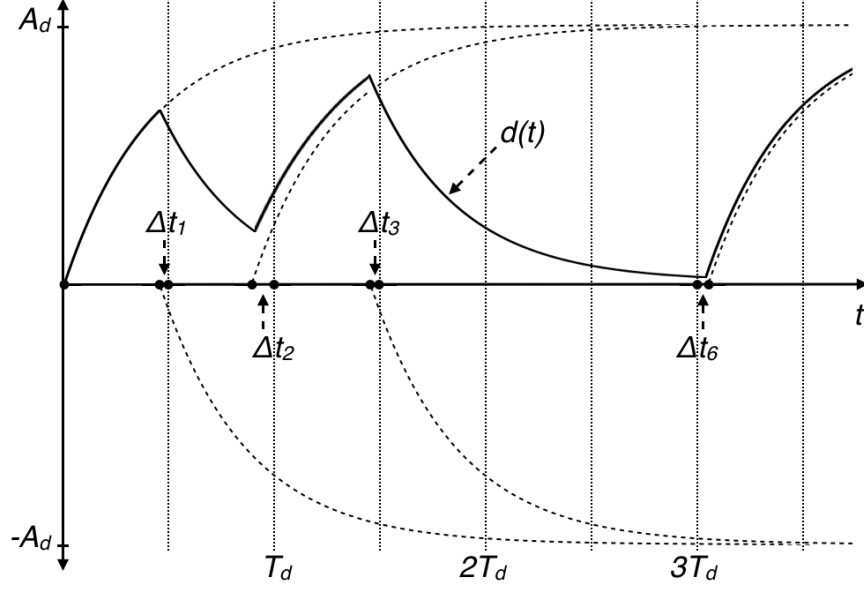
$$s(t_i) = \cos\left(\frac{2\pi}{T_d} \cdot t_i + \Delta\phi_d(t_i)\right) = 0. \quad (9)$$

To understand the proposed model, jitter modeling for the bit sequence 10100011 is illustrated in Figure 4. Each element of the series in Equation 1 is represented by the dotted line, and the resultant waveform  $d(t)$  is depicted by the solid line. Note that the timing error values, applied to the bit sequence, are set relatively large and fast-varying for presentation purpose.

## 2.2 Time-Domain Jitter Expansion Sensor

### 2.2.1 Overview

The proposed configuration enables a low-speed jitter test environment. In this approach, the timing error of a high-speed signal is characterized using a special circuit

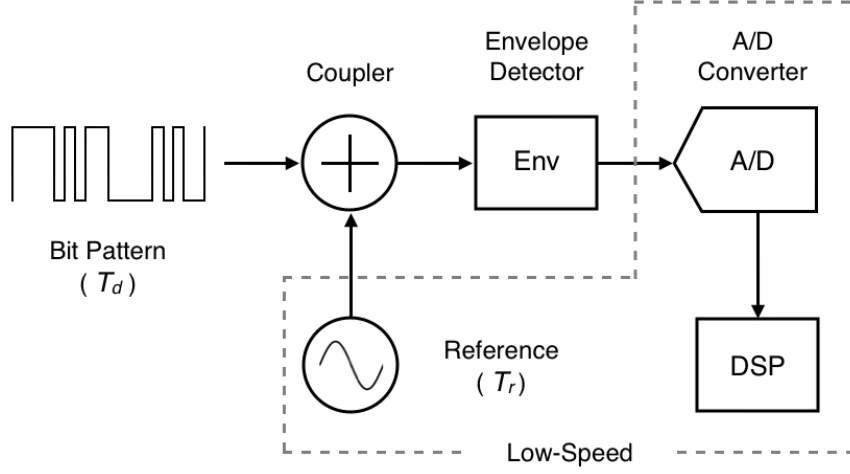


**Figure 4:** Illustrated formulation of the bit pattern 10100011 with jitter, based on the model described in Section 2.1.

called a jitter sensor, which produces a low-speed output signal with expanded jitter (jitter of the high-speed signal amplified by a constant scaling factor). The reference signal required by the jitter sensor is a low noise (stable), low-frequency sinusoidal signal. A narrow-bandwidth, low-speed (multi-Msps) digitizer is used to acquire the sensor output signal.

The proposed jitter test configuration is shown in Figure 5. The sinusoidal reference signal has a frequency much lower than that of the bit pattern being tested. This reference signal need not be synchronized with the bit pattern in time but should be slightly offset in frequency. The bit pattern to be tested and the reference signal are fed to the RF power combiner. Due to the frequency offset between the two signals, the combined signal has a slow-varying envelope, whose frequency is determined by the bit frequency. The coupled signal is subsequently fed to the proposed jitter sensor. The operation of this sensor circuit is based on envelope detection and resultant frequency down-conversion. The output signal of the sensor is in the baseband and





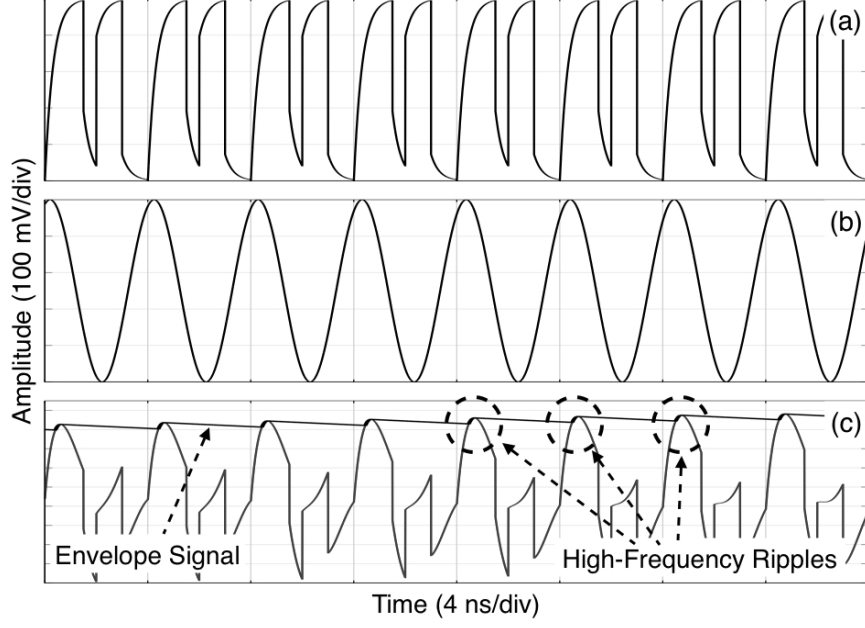
**Figure 5:** Proposed test setup for jitter expansion of high-speed digital signals: The low-speed signal area is denoted by the dotted line.

contains the original jitter information. The sensor output signal can be analyzed using a narrow-bandwidth, low-speed digitizer and then processed using a digital signal processor (DSP) to determine the jitter value of the original high-speed signal.

### 2.2.2 Low-Speed Reference Signal

Most electrical test and measurement instruments require either internal or external references which need to be stable. In the proposed jitter test configuration, a sinusoidal reference signal with reduced frequency is utilized so that the reference signal can be supplied with less concern for additive noise and distortions. With regard to phase stability, such a low-speed reference signal can be generated from standard test instruments with less phase noise compared to that of the high-speed counterpart. This is because the relative phase noise of an oscillator is proportional to the square of its operation frequency [49]. Another advantage of using the low-frequency sinusoidal reference signal is that, compared to higher speed sinusoidal or digital signals, the low-frequency signals produce greater noise robustness and are easier to generate.

In terms of noise robustness and ease of generation, the low-frequency sinusoidal reference signal is advantageous compared to other types of reference signals such as



**Figure 6:** Waveforms at each functional nodes: (a) the bit stream of 11101100, (b) the sinusoidal reference signal, and (c) the combined signal and its envelope tracking.

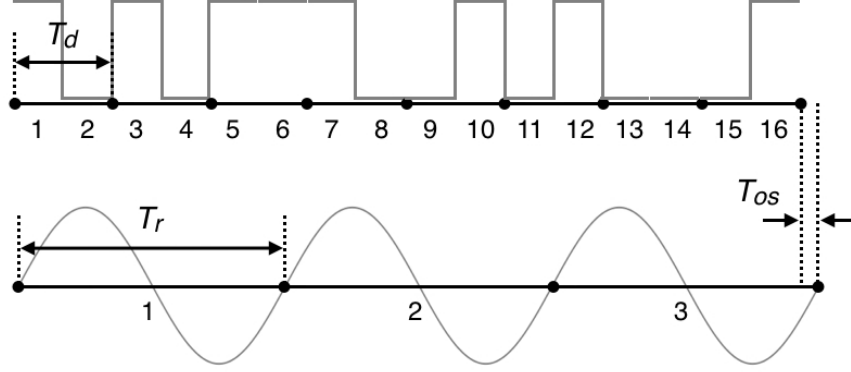
at-speed (or high-speed) sinusoidal or digital signals.

The reference signal  $r(t)$  is given by:

$$r(t) = A_r \cdot \cos\left(\frac{2\pi}{T_r} \cdot t\right), \quad (10)$$

$$\beta \cdot T_r = \alpha \cdot T_d/2 + T_{os} \quad (11)$$

where  $A_r$  is the reference signal amplitude,  $T_r$  is the reference signal period,  $\alpha$  and  $\beta$  are the integer scalars, and  $T_{os}$  is the period offset value. Figure 7 shows the case with  $\alpha=l=16$  and  $\beta=3$  ( $l$  denotes the bit pattern length). Likewise, by selecting the values of  $\alpha$  and  $\beta$ , a small value of  $T_{os}$  can be derived so that the envelope frequency of the combined signal is low. Note that  $T_{os}$  defines the envelope frequency of the combined signal as described in Section 2.2.3. The  $T_{os}$  value, however, does not have to be accurate as it is not related to the accuracy of jitter measurement. This flexible setup alleviates synchronization requirements between the input test pattern and the reference signal. In general,  $\alpha$  can be the same as the length of the input test pattern.



**Figure 7:** An example setup of the period offset  $T_{os}$  with  $\alpha=l=16$ ,  $\beta=3$ .

### 2.2.3 Time-Domain Jitter Expansion

The proposed jitter sensor performs jitter expansion by converting a high-speed input signal to a low-speed output signal with amplified jitter (as defined later by the jitter expansion ratio). Figure 6 shows waveforms corresponding to the circuit nodes of Figure 5, and gives the digital signal to be analyzed for jitter as a bit sequence 11101100 and the reference signal as a low-frequency sinusoid ( $\beta=1$ ,  $\alpha=l=8$ ). These two signals are combined and fed to the input of the jitter sensor. The jitter sensor then generates the envelope of the combined signal as an output signal. Figure 6-(c) shows the combined signal and the sensor output (envelope) signal.

The envelope signal period  $T_e$  is determined by the two input signal period values ( $T_d$ ,  $T_r$ ) and their offset period value ( $T_{os}$ ) as described by Equations 10 and 11. Due to the offset  $T_{os}$ , the two input signals continuously shift (in time) against each other. After a certain amount of time shift, the two periodic signals coincide in terms of signal phase, synchronization which occurs periodically. This periodicity determines the envelope signal period  $T_e$  as shown below (in the case of  $\beta = 1$  or  $\alpha = l$ ).

$$T_e = \frac{T_r \cdot l \cdot T_d / 2}{|T_{os}|}. \quad (12)$$

When the value of  $T_{os}$  is small compared to that of  $T_d$  and  $T_r$ , the sensor output signal (envelope signal) is at low speed. Note that this formula assumes that the

digital signal being tested contains no timing noise.

In cases where the digital signal contains random jitter, the resulting envelope signal fluctuates in time, and the envelop signal fluctuation (jitter) correlates with the original digital signal jitter. In Figure 8, computer simulation is used to compare an envelope signal with jitter to a jitter-free envelope signal (assuming a jitter-free input digital signal). The jitter-free envelope signal is deterministic. In contrast, the envelope signal with jitter shows random fluctuations that contain the jitter information of the signal being tested. In other words, the envelope signal period  $T_e$  is time-varying due to the input digital signal jitter. The time-varying (or random) value of  $T_e$  is analyzed in terms of timing noise, and the jitter information of the signal being tested can be indirectly extracted from the envelope signal.

The envelope signal jitter is the expanded version of the original digital signal jitter. The envelope signal jitter's expansion ratio  $\lambda$ , which needs to be determined, is defined below.

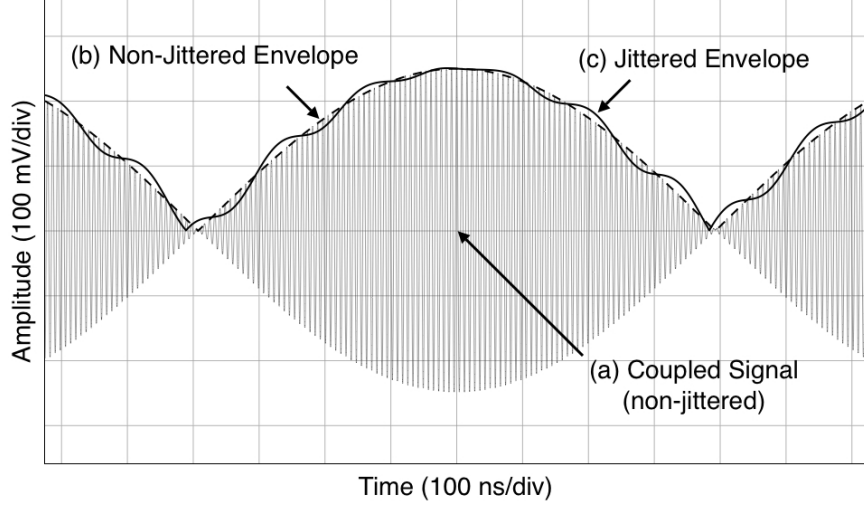
$$\lambda = \begin{cases} T_e / (l \cdot \frac{T_d}{2}) = T_r / |T_{os}| & \beta = 1, \\ T_e / T_r = l \cdot \frac{T_d}{2} / |T_{os}| & \alpha = l. \end{cases} \quad (13)$$

Once the value of  $\lambda$  is calculated and the envelope signal jitter is measured, the original digital signal jitter value can be estimated. A detailed analysis of jitter expansion is given in Appendix A.

Using computer simulation, a 2-Gbps bit pattern of 11101100 with jitter (generated based on Equations 1-9) and a noiseless 249-MHz reference sinusoid were generated ( $\alpha = l = 8$ ,  $\beta = 1$ ), and the envelope function of the combined waveform was derived by tracking the voltage peaks. The simulation results are shown in Figure 9. Plot (a) shows the input bit pattern 11101100 with 10.00 psec rms random jitter, and plot (b) depicts the resulting 1-MHz sensor output (envelope) signal with expanded jitter of 2.49 nsec rms.<sup>1</sup> The simulated jitter expansion factor is in agreement with

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<sup>1</sup>The simulation result was originally provided in [15].



**Figure 8:** Illustration of the signals at each functional node: (a) a combined signal (digital clock signal + sinusoidal reference signal), (b) an envelope signal without jitter, (c) an envelope signal with jitter, containing jitter-induced voltage fluctuation.

the jitter expansion ratio  $\lambda$  of 249 (calculated based on Equation 13).

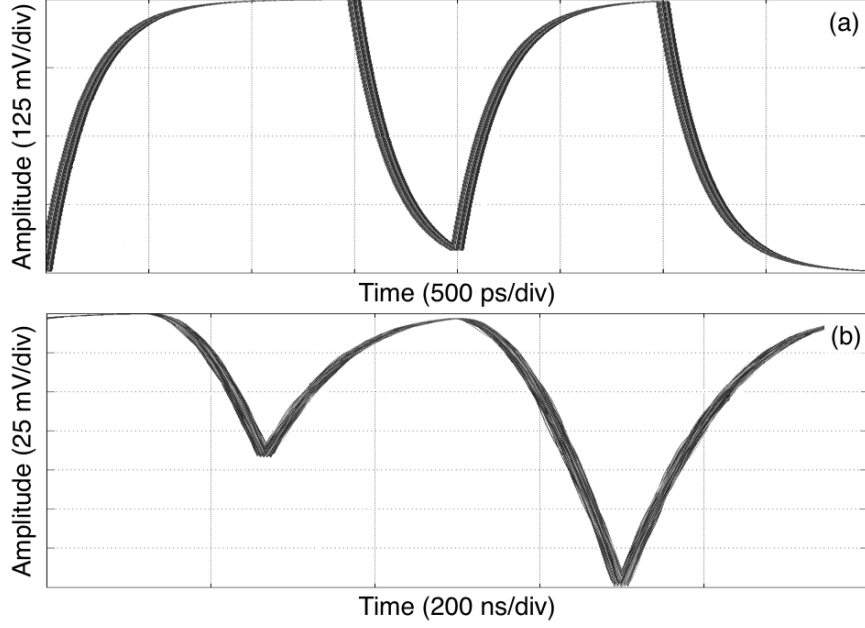
#### 2.2.4 Low-Speed Signal Acquisition

The jitter sensor output signal (or envelope signal) obtained in Section 2.2.3 can be acquired with low-speed data converters or low-frequency spectrum analyzers (The frequency requirement for the instrument is multi-MHz, rather than multi-GHz). These low-speed measurements alleviate measurement errors that may occur when the signal is measured with high-speed jitter analyzers due to non-idealities of high-speed signaling and acquisition. The hardware validation to be described later in Section 2.4 shows the accuracy of the sensor output acquisitions with low-speed digitizers (or oscilloscopes).

### 2.3 Practical Considerations

#### 2.3.1 Jitter Bandwidth of Interest

We assume that the phase-noise (or jitter) bandwidth of interest is practically limited up to the offset frequency of 100-MHz. According to the phase noise model in [22], voltage noise applied to an electrical oscillator results in wideband phase noise at



**Figure 9:** Simulation results shown in the accumulative plot: (a) the 11101100 digital signal being tested and (b) the corresponding jitter-sensor output signal. Note that the time-scale of (a) is different from that of (b).

the output signal of the oscillator. However, the far-out phase noise over 100-MHz offset frequency is usually overwhelmed by the noise floor of the generated signal. In addition, such very far-out phase noise power may be too low to be measured using sampling-based equipment. For these reasons, in the proposed jitter testing setup, the jitter sensor is used to derive the output signal with the bandwidth of 100-MHz, and accordingly incorporates the phase noise up to 100-MHz offset frequency.

To reduce undesired noise, a low-pass filter is used at the output of the sensor. The output envelope signal of the jitter sensor contains high-frequency ripples in the extracted envelope, as illustrated in Figure 6-(c). These ripple components are by-products obtained in the envelope detection by the charge-pump circuit of the jitter sensor. With regard to jitter information (which is detected by the jitter sensor), these ripple components behave like additive noise. Thus, a low-pass filter, whose cutoff frequency is slightly beyond the jitter bandwidth of interest, can be applied to the output of the sensor to eliminate high-frequency ripples of Figure 6-(c). This

filtering does not remove jitter content in the sensor output signal.

### 2.3.2 Jitter in the Reference Signal

This section briefly discusses the relation between the frequency of an oscillator and the amount of its phase noise. Noise components in the reference signal (utilized for the jitter sensor) degrade the test accuracy of the proposed jitter testing technique. The jitter sensor scales (expands) the input digital signal jitter being tested and the reference signal jitter concurrently by a factor given by the expansion ratio  $\lambda$  (where  $\lambda \gg 1$ ). Even with the low-speed reference signal (required for the jitter sensor), the residual jitter of the reference signal affects the overall jitter testing accuracy. Thus, the reference signal jitter needs to be analyzed carefully.

The relative phase noise of a (reference) voltage-controlled oscillator (VCO) is modeled as a function of its operation frequency in [32, 49]:

$$L_\phi(\Delta\omega) \propto \left(\frac{\omega_r}{\Delta\omega}\right)^2 \frac{1}{V_{sw}^2} \frac{1}{I_{dd}} \quad (14)$$

where  $L_\phi$ ,  $\Delta\omega$ ,  $V_{sw}$  and  $I_{dd}$  denote respectively the relative phase noise, offset frequency, internal voltage swing, and total supply current. This equation shows that the power spectrum of the phase noise is proportional to the square of  $\omega_r$ . Accordingly, an oscillator with lower operation frequency shows better phase noise performance. The relation between the timing error  $\Delta t_r$  and the phase noise  $\Delta\phi_r$  is determined by

$$\Delta t_r(t) = \frac{\Delta\phi_r(t)}{\omega_r} \quad (15)$$

where  $\omega_r = 2\pi/T_r$ . From Equations 14 and 15, it is evident that the jitter performance of an oscillator does not change with the value of the operation frequency  $\omega_r$  even though lower operation frequency results in better phase noise performance.

Since the reference signal is of lower frequency as compared to the test signal, even though it might have jitter characteristics similar to its high-speed counterparts, it is relatively much more robust at dealing with noise and distortion induced by non-ideal transmission channels.

### 2.3.3 Additive Noise Compensation

Due to non-idealities in the jitter sensor, the measured jitter value can be corrupted by additive noise induced by the reference oscillator, combiner, and envelope detector. To compensate for additive measurement noise, the jitter sensor must be calibrated prior to jitter testing. We assume that additive measurement noise is uncorrelated with noise (or jitter) of the input digital signal being tested. The compensation procedure is based on the formula below.

$$\Delta t_e = \lambda \cdot \sqrt{\Delta t_d^2 + \Delta t_m^2}. \quad (16)$$

where  $\Delta t_d$  and  $\Delta t_e$  are the root mean square (rms) jitter values of the input digital signal and the output envelope signal (of the jitter sensor), respectively.  $\Delta t_m$  is the pre-characterized value of additive measurement noise (represented as a rms jitter value) as determined with a spectrum analyzer.

The noise compensation technique is used in hardware validation (Section 2.4.1.1). As shown in Figure 14(a) and Figure 14(b), noise compensation enhances the overall jitter test resolution.

### 2.3.4 Nonlinear Responses of the Jitter Sensor

Due to its nonlinearities, the jitter sensor produces harmonic components, but these harmonic terms do not negatively affect the accuracy of the jitter test. Since the response of the jitter sensor (envelope extraction) to the input (combined) signal is inherently time-varying and nonlinear, the sensor output signal contains multiple harmonics of the fundamental bit frequency  $1/T_e$ . The nonlinearity can be expressed in a closed-form formula if the input digital signal with jitter is modeled as (or simplified to) a sinusoid  $d_s(t)$  with phase noise.

$$d_s(t) = A_d \cdot \cos\left(\frac{2\pi}{T_d} \cdot t + \Delta\phi_d(t)\right). \quad (17)$$



The reference signal is modeled based on Equation 10 and Equation 11 ( $\alpha=2, \beta=1$ ). Assuming that the envelope extraction is perfectly performed by the jitter sensor, no high-frequency ripple components remain at the envelope signal. The sensor output signal is represented as below.

$$e(t) = \sqrt{A_d^2 + A_r^2 + 2A_dA_r \cdot \cos(\omega_{os}t + \Delta\phi_d(t))}, \quad (18)$$

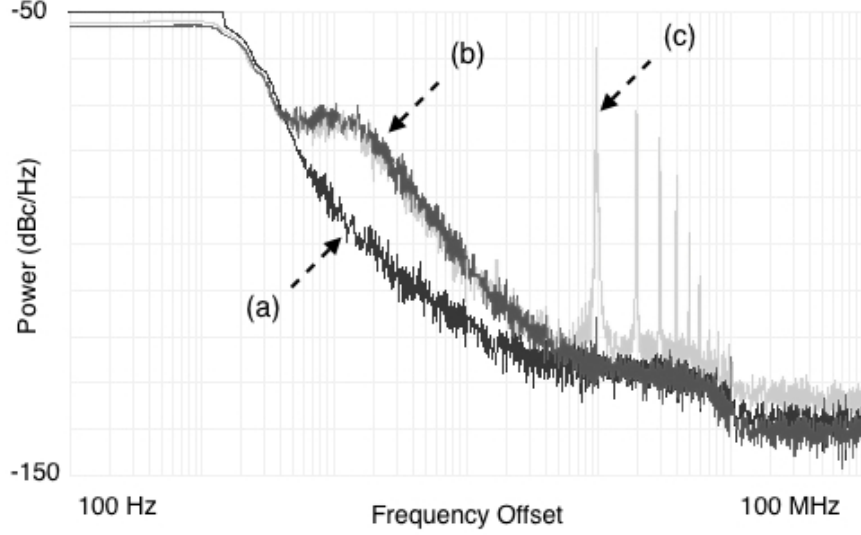
$$\omega_{os} = \frac{2\pi}{T_d} - \frac{2\pi}{T_d + T_{os}} \quad (19)$$

where  $\omega_{os}$  is the offset angular frequency. The  $e(t)$  is a rectified cosine function. In other words, the  $e(t)$  consists of an infinite series of cosine harmonics. Accordingly,  $e(t)$  can be rewritten.

$$e(t) = \sum_{k=1}^{\infty} A_k \cdot \cos(k \cdot \omega_{os}t + k \cdot \Delta\phi_d(t)) + A_0 \quad (20)$$

where  $A_k$  is the amplitude of the  $k$ -th order harmonic. Note that the phase noise term  $\Delta\phi_d(t)$  is concurrently applied to all the harmonic components, and accordingly the phase noise values of all the harmonic components (including the fundamental tone) are synchronized in time. Thus, the harmonic components due to nonlinearities in the jitter sensor do not introduce additional jitter into the sensor output signal.

To support the above argument, we conducted frequency-domain and time-domain measurements, comparing the two measurement results against each other. First, the power spectra of the signal nodes in Figure 5 were obtained using a spectrum (phase noise) analyzer (Agilent E4407B). Figure 10 shows the phase noise spectra of (a) a 2.401-GHz reference sinusoid generated by a signal generator (Agilent E4432B), (b) a 2.4-GHz signal under test derived from an integrated phase-locked loop (PLL) & voltage controlled oscillator (VCO) frequency synthesizer (Analog Devices EVAL-ADF4360), and (c) the resultant 1-MHz jitter sensor output signal. These three phase noise spectra are overlapped on the same figure for comparison. Spectrum (b) shows a phase noise value of -73 dBc/Hz at 10-kHz offset and -105 dBc/Hz at 100-kHz offset

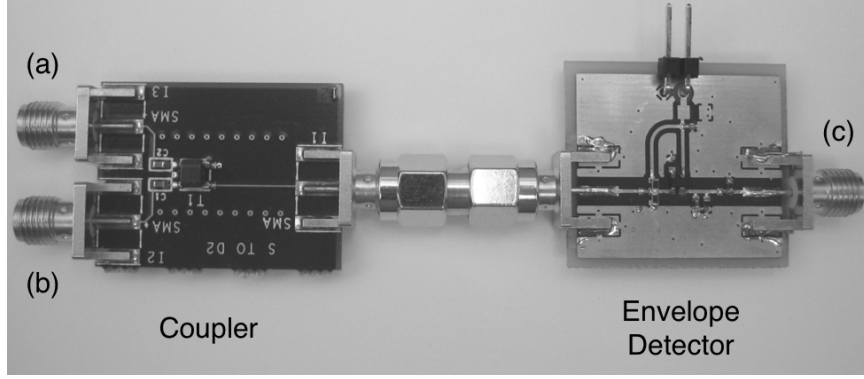


**Figure 10:** Overlapped phase-noise plot: (a) the 2.401-GHz reference sinusoid, (b) the 2.4-GHz phase-noisy signal being tested, and (c) the 1-MHz envelope signal at the output of the jitter sensor.

due to the frequency synthesizer's inherent phase noise being measured by the jitter sensor. Spectrum (c) is a low-frequency replica of spectrum (b) (jitter expansion), but contains additional harmonic components. For reference, a time-domain measurement is performed. Then, the contribution of the additional harmonic components, those in spectrum (c), to the overall jitter value is determined. With a digital oscilloscope (Agilent E8257D PSG), the jitter values of signals (a), (b) and (c) measure 0.218 psec rms, 1.878 psec rms and 1.895 nsec rms, respectively. Note that the jitter value of (c) is  $\approx 1002$  times the rms sum of the jitter values of (a) and (b) when the calculated value of  $\lambda$  is 1000 (The small error in jitter expansion is due to additive measurement noise). The results of our frequency and time-domain experiments suggest that the harmonic terms do not contribute to the overall jitter and that the inherent nonlinearity of the jitter sensor does not generate additional jitter noise.

## 2.4 Validation

To supplement the simulation results, this section presents an experimental validation of the proposed jitter expansion technique. Section 2.4.1.1 evaluates the linearity of



**Figure 11:** Picture of the RF power combiner and jitter-sensor: (a) the combiner input for the reference signal, (b) the combiner input for the digital signal being tested, and (c) the output of the jitter sensor.

jitter expansion. Section 2.4.1.2 describes how the jitter of a  $K28.5 \pm$  bit pattern is expanded and measured using an digital oscilloscope. In Section 2.4.2, the test resolution of the jitter sensor is evaluated using a low-speed digitizer.

#### 2.4.1 Linearity of Jitter Expansion

The linearity of jitter expansion was evaluated using hardware experiments. For the experiments, the jitter sensor was implemented on a printed circuit board (PCB) as shown in Figure 11. To generate a high-speed bit pattern with various amount of jitter, we used a digital transmitter (HP 70843B), and phase modulated its time-base signal (jitter injection) by using an additional signal generator (Agilent E4432B). Another signal generator (Agilent E4433B) generated a sinusoidal reference signal. Note that it was necessary to synchronize these three signal generators in frequency. The jitter sensor output signal was acquired by a digital oscilloscope (Agilent Infiniium DCA 86100A) and a low-speed digitizer.

##### 2.4.1.1 Clock Test Pattern

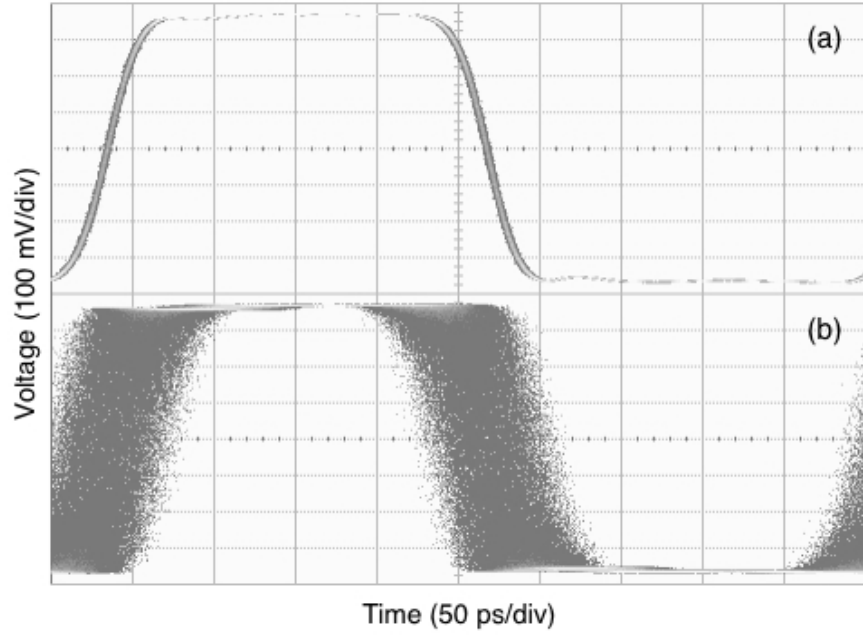
To test jitter of a 2-GHz digital clock signal, a 500.5-MHz reference sinusoidal signal was applied to the jitter sensor ( $\alpha=8$ ,  $\beta=1$ ,  $l=2$ ,  $T_{os} \approx 2$  psec). To experiment with various amount of clock jitter, the random jitter of 0 psec rms to 17 psec rms was

injected into the clock signal (using the previously described jitter injection setup). While the various values of clock jitter were being injected, the corresponding sensor output signal jitter (the expanded version of the injected jitter) was measured with the digital oscilloscope. In Figure 12(a), the oscilloscope measurement (eye-diagram mode) results for the digital clock signal without and with jitter injection (17 psec rms) are shown at (a) and (b) respectively. Figure 12(b) shows the corresponding sensor output signals. The jitter values of plots (a) and (b) in Figure 12(b) measure 6.68 nsec rms and 17.95 nsec rms, respectively. Compared to plot (b) in Figure 12(a), plot (b) in Figure 12(b) shows that the injected jitter has expanded  $\approx 1056$  times by the jitter sensor. In comparison, the calculated jitter expansion ratio  $\lambda$  is 1000. Such an error in jitter expansion ratio is due to additive measurement noise, but it can be compensated for by using the additive noise compensation technique described in Section 2.3.3.

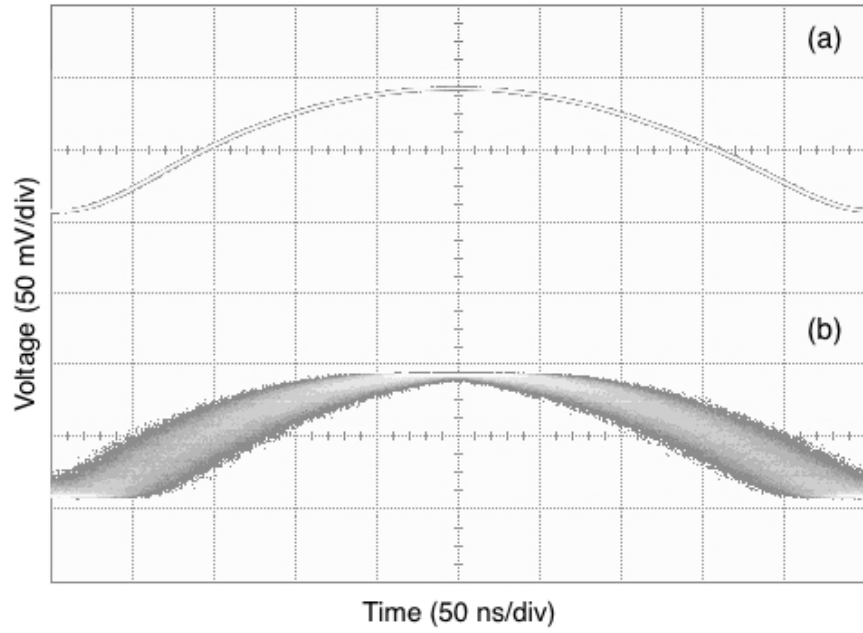
The linearity of jitter expansion was evaluated by using 15 incremental values of injected jitter from 0 psec rms to 8.5 psec rms. The  $\underline{x}$ 's in Figure 14(a) denote the plot for the injected clock jitter values versus the expanded jitter values, which are measured from the sensor output signal. The expanded jitter measures are compensated for additive measurement noise based on Equation 16, and the compensated results are denoted by  $\underline{o}$ . The linearity of jitter expansion is determined by comparing the compensated results to the linear slope plot (denoted by a dotted line). The rms error of the jitter expansion measures 0.2797 nsec rms in the expanded time scale (or 0.2797 psec rms in the original time scale).

#### 2.4.1.2 K28.5± Test Pattern

This section details how the jitter sensor was used to test jitter of a K28.5± bit pattern 11111010110000010100 (a common stimulus in testing fiber channels or Ethernet systems). A 2-Gbps K28.5± pattern was generated with random jitter injection up

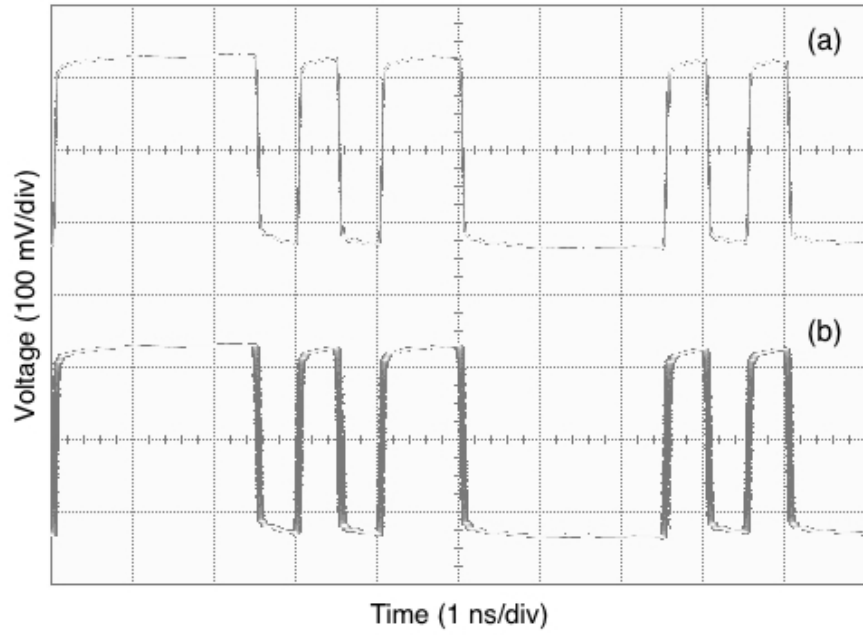


(a) Plot (a) indicates a 2-GHz clock signal without injected jitter, and plot (b) denotes a 2-GHz clock signal with 8.5 psec rms random jitter injected.

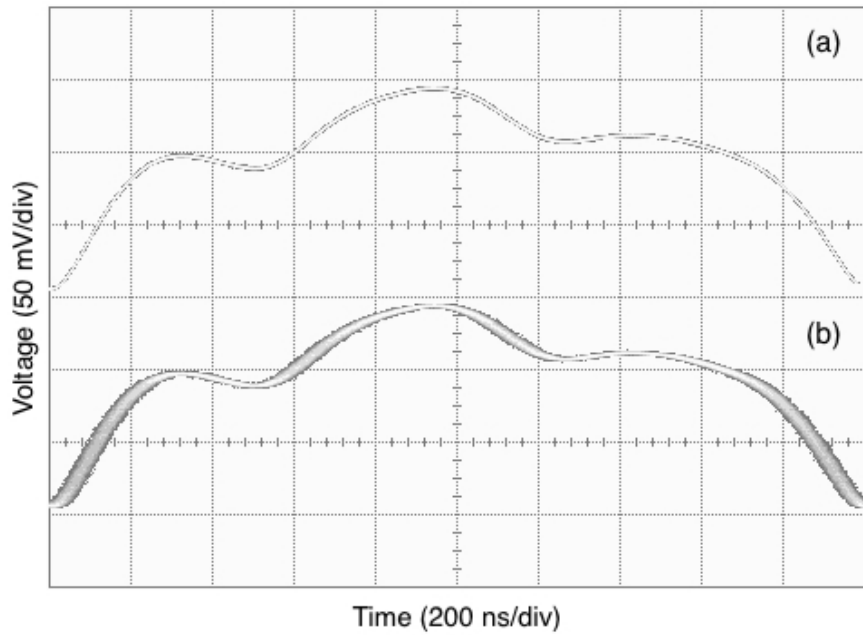


(b) Plot (a) indicates the sensor output signal corresponding to Figure 12(a)–(a), and plot (b) denotes the sensor output signal corresponding to Figure 12(a)–(b).

**Figure 12:** Oscilloscope measurements of clock signal jitter.

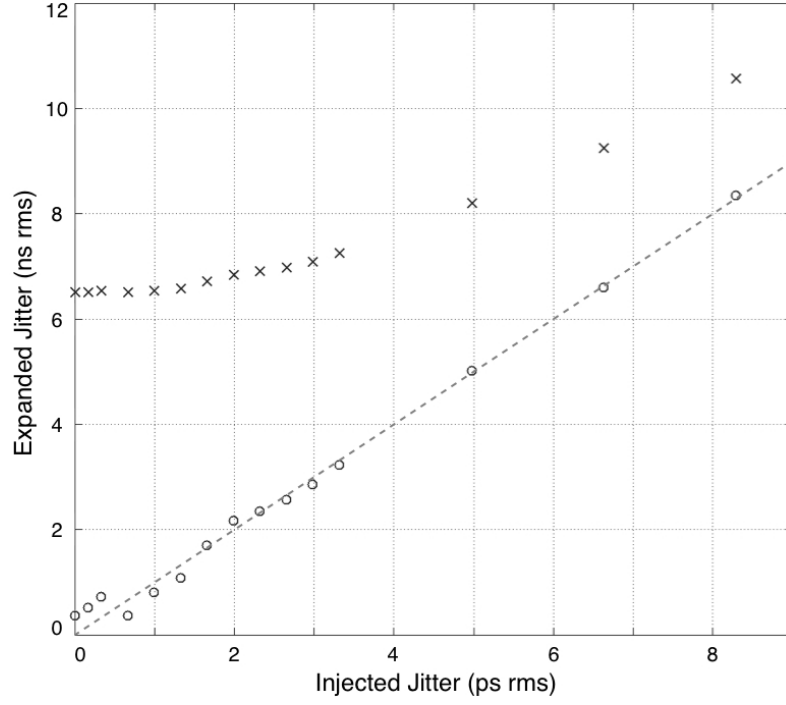


(a) Plot (a) indicates a 2-Gbps K28.5± pattern signal without injected jitter, and plot (b) denotes a 2-Gbps K28.5± pattern signal with 17 psec rms random jitter injected.

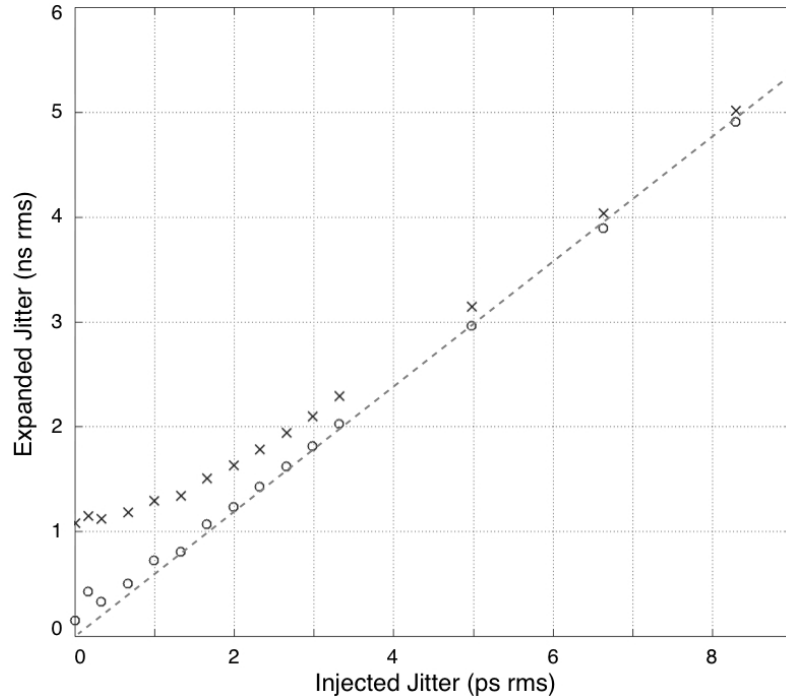


(b) Plot (a) indicates the sensor output signal corresponding to Figure 13(a)–(a), and plot (b) denotes the sensor output signal corresponding to Figure 13(a)–(b).

**Figure 13:** Oscilloscope measurements of digital signal jitter.



(a) Jitter expansion of 2-GHz digital clock signals: o's and x's respectively denote the measurement results with and without incorporating the measurement noise compensation.



(b) Jitter expansion of 2-Gbps K28.5± pattern signals: o's and x's respectively denote the measurement results with and without incorporating the measurement noise compensation.

**Figure 14:** Linearity measurements of jitter expansion.

to 17 psec rms, and a 300.5-MHz sinusoid was used as a reference signal ( $\alpha=20$ ,  $\beta=3$ ,  $l=20$ ,  $T_{os}\approx 16.6$  psec). The direct oscilloscope measurements of the bit pattern without and with jitter injection (17 psec rms) are shown at (a) and (b) in Figure 13(a), and the corresponding sensor output signals are shown at (a) and (b) in Figure 13(b), respectively. The rms jitter values of the sensor output signal (a) and (b) measure 1.08 nsec rms and 10.23 nsec rms, respectively. The injected jitter expanded  $\approx 601.8$  times (before the additive noise compensation). This measured jitter expansion ratio is very close to the calculated value of 600.

The linearity measurement of jitter expansion is shown in Figure 14(b) for the  $K28.5\pm$  pattern signal with injected jitter up to 8.5 psec rms. The measurement results are denoted as  $\underline{x}$ , and their post-compensated values are shown as  $\underline{o}$ . The rms error of the compensated values compared to the dotted reference line is 0.1091 nsec rms in the expanded time scale, which is the same as 0.1818 psec rms in the original time scale.

#### 2.4.2 Jitter Test Accuracy

To evaluate the test resolution of the jitter sensor with a low-speed digitizer, we used the Alazartech ATS460 digitizer (14-Bit, 125 MS/s) as a substitute for the digital oscilloscope (for the sensor output signal acquisition). The rest of the experimental configuration was the same as in Section 2.4.1. A 2.8-Gbps 11011100 bit pattern and a 351-MHz sinusoid were used respectively as a signal being tested and a reference signal ( $\alpha=l=8$ ,  $\beta=1$ ). Figure 15(a) shows the digitizer capture of the sensor output signals: (a) without injected jitter and (b) with 1 psec rms jitter injected. The 1 psec rms jitter injection results in a visible distinction (phase dispersion) of the sensor output signal. Thus, the test resolution of the jitter sensor in this particular evaluation setup is at least 1 psec rms (in the original time scale).

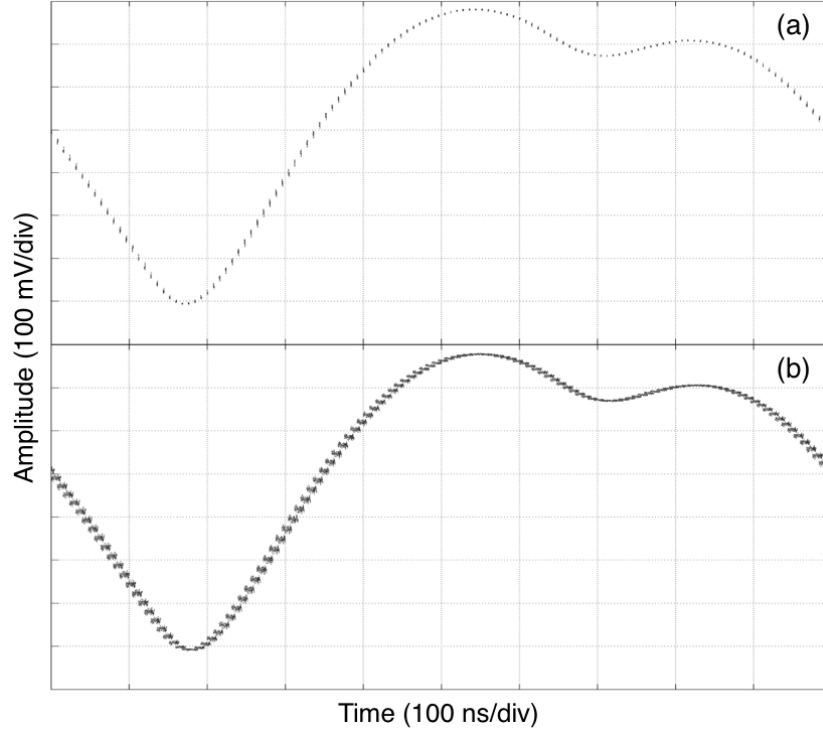
Another evaluation of the jitter test accuracy of the jitter sensor was performed



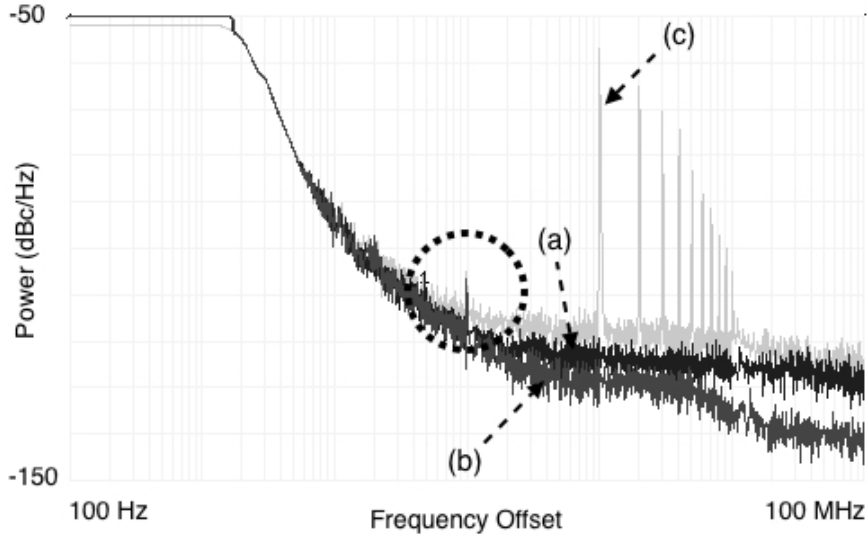
with a spectrum analyzer. A 2.4-GHz phase-modulated sinusoidal signal being tested was generated as denoted by (b) in Figure 15(b). The use of a sinusoidal signal, instead of a digital signal, was because a digital signal could be hardly observed with a spectrum analyzer due to the signal's complex spectrum. The phase-modulation signal was given by a 0.002 rad, 100-KHz sinusoid to mimic phase noise (or jitter). A 2.401-GHz sinusoidal signal was used as a reference signal, as denoted by (a) in Figure 15(b) (However, a lower frequency reference signal can be also used). The envelope signal obtained by the jitter sensor was fed to the spectrum analyzer to measure the phase noise of the signal, as denoted by (c) in Figure 15(b), which shows that the envelope signal's phase noise content, which originates from the 0.002 rad sinusoidal phase modulation of the signal being tested, is detectable with the spectrum analyzer.

## 2.5 Summary

This chapter presents a method of time-domain jitter expansion, which is applicable to testing jitter of digital bit sequences with low-speed testers. The frequency of the reference signal can be multiple times lower than that of the digital signal being tested. A low-speed envelope signal with expanded jitter is generated by the jitter sensor and then acquired by a low-speed digitizer. The hardware results show the jitter test resolution of the jitter sensor is 1 psec rms.



(a) Digitizer capture of envelope signals: plots (a) and (b) respectively denote the envelope signals without and with jitter injection (1 psec rms jitter).



(b) Phase noise measurements: plots (a), (b) and (c) respectively denote the spectra of the 2.401-GHz sinusoidal reference signal, 2.4-GHz sinusoidal signal being tested (with 0.002 rad, 100-KHz sinusoidal phase modulation), and 1-MHz envelope signal.

**Figure 15:** Jitter test accuracy evaluation of the jitter expansion sensor.

## CHAPTER III

### SIMPLIFIED DIRECT DIGITIZATION TECHNIQUE USING INCOHERENT SUB-SAMPLING

A sampling-based signal acquisition device is frequently utilized for high-speed signal measurement and characterization. The sampling rate of such instrumentation is, however, limited in practice. Overcoming such a limitation requires high-speed digital oscilloscopes equipped with equivalent-time sampling functions, which employ a fixed frequency sampling clock combined with a swept delay circuit [42]. The digitizer captures the horizontal sweep of a periodic waveform at a relatively low sampling speed. Timing information is obtained from the swept delay circuit, and the digitized samples are processed digitally to re-build the signal for a single cycle. In this sampling technique, the accuracy of the swept delay line is critical for minimizing measurement timing error. However, due to imperfections in the delay circuitry, it is possible that nonlinearity and random errors are introduced into the delay time; consequently, these timing errors degrade the measurement accuracy. Another approach to digitizing high speed signals using low speed clocking mechanisms is the use of parallel sampling architecture. In this architecture, multiple samplers are used in parallel to digitize the common analog signal using independent sampling clocks that contain a dedicated timing delay. In [45], a total real-time sampling rate of 20-Gsps was achieved. In the parallel sampling method, imperfections in the multiple delay lines degrade the measurement resolution in the same manner as equivalent-time sampling.

For high-speed signal spectral analysis, coherent sub-sampling is utilized [4, 8, 19, 29, 35, 36, 46, 48]. In this approach, an analog waveform is digitized over an integer number of cycles (coherency) at a sampling speed which is lower than the Nyquist

rate [40, 54]. Coherent sampling eliminates unwanted discontinuities in sampled signals and minimizes the spectral leakage of the signals in the frequency domain. However, the coherent sub-sampling method (for spectral analysis) has limitations. First, enabling coherency requires additional hardware to synchronize the analog signal being sampled with the sampling clock. The use of the synchronization hardware complicates the validation of the sampling system. Second, spectral content outside the sampling bandwidth is aliased, so the analog frequency information of the sub-sampled signal is lost unless the frequency of the sub-sampled signal is known precisely and the sub-sampling rate is adjusted to accommodate for that. Finally, infrequent glitches and timing noise in the signal are hard to observe in spectrum analysis due to its averaged power measurement.

In contrast to the coherent sub-sampling based spectral measurement, a time-domain measurement using incoherent sub-sampling is presented in this chapter. First, the proposed back-end signal reconstruction algorithms are used to re-map a raw incoherently sub-sampled signal in order to represent the signal within its single cycle (in the discrete time domain). Note that the proposed signal acquisition technique does not require timing circuitry such as a delay line or a synchronization module: such hardware-based timing functions are replaced by digital processing algorithms, which do not require the use of additional analog hardware. From the reconstructed waveform in the discrete time domain, signal parameters such as rise/fall time, pulse width/height, signal overshoot/undershoot, and ringing can be determined for test and measurement purposes (However, these parameters are not evaluated in this dissertation). Random timing noise of the signal can also be observed in the discrete time domain. Spectral leakage related measurement inaccuracy due to incoherent sampling can be overcome using digital signal processing. In addition, if the sampling speed is switched, the analog frequency value can be recovered from sampled signals. The analog frequency information of sub-sampled signals is,

otherwise, lost due to spectrum aliasing distortion.

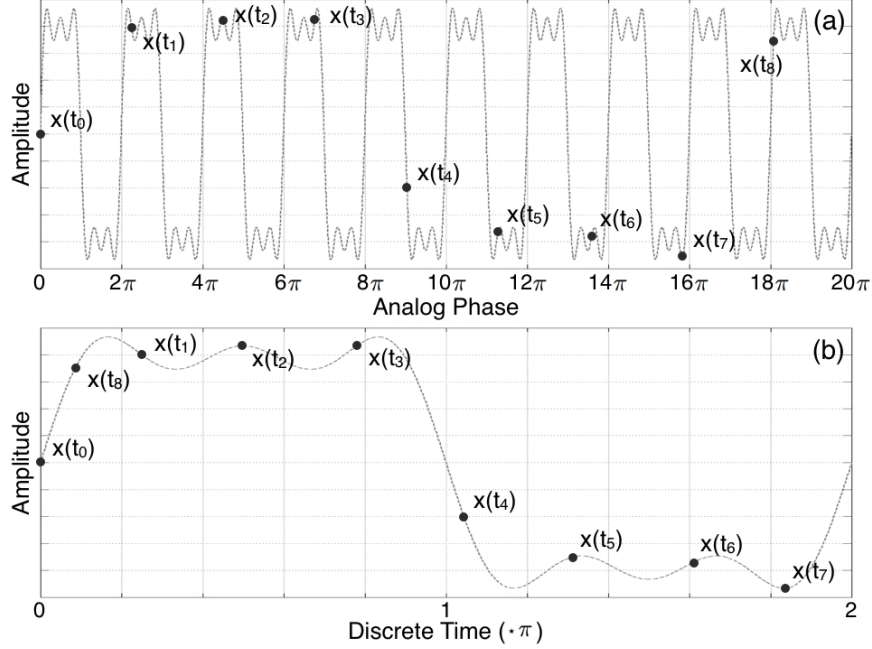
The aim of this work is to provide a first proof-of-concept for the simplification of the conventional signal acquisition systems by using less number of RF/mixed-signal circuits compared to traditional sampling-based signal analyzers. The proposed method does not use timing circuitry (for synchronization) such as a delay generator, time-to-digital converter and hardware clock recovery unit. The core innovations of the signal acquisition technique proposed in this chapter include:

- a simplified signal acquisition architecture in terms of RF/mixed-signal designs.
- software implementation of time synchronization hardware used in traditional digital oscilloscopes.
- possible reduced measurement and test cost due to their ease of deployment and simplicity (further investigation is needed to project whether this approach would alleviate the cost of production test).

## 3.1 Simplified Signal Acquisition Architecture

### 3.1.1 Incoherent Sub-Sampling

A high-speed periodic signal, whose operation frequency is higher than half the sampling rate of the digitizer, is *incoherently sub-sampled* at a fixed rate. As shown in Figure 16-(a), the data points of the sub-sampled signal are coarsely distributed in time. Even though the time resolution of the sampled signal is not enough to completely reconstruct its real-time waveform—the Nyquist sampling criteria, the sub-sampled signal can be reconstructed in non-real-time, where the samples are re-mapped to the discrete time domain  $[0, 2\pi]$  as illustrated in Figure 16-(b). Each sample point contributes to re-building the waveform in the equivalent-time sense. For such signal re-mapping, standard instrumentation utilizes additional hardware such as delay and trigger signal generators. In the proposed approach, however, the signal re-mapping is



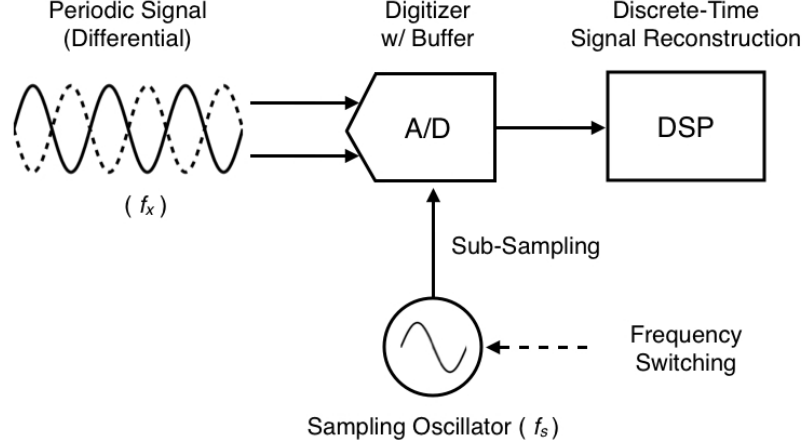
**Figure 16:** Time re-mapping of an incoherently sub-sampled signal: (a) an analog periodic signal shown with its sampled data (in the raw sequence), and (b) the reconstructed waveform with the re-mapped samples in the discrete time domain.

enabled by the software-based signal reconstruction (to be described in the following section).

As shown in Figure 17, the proposed incoherent sub-sampling and signal reconstruction setup consists of an analog-to-digital converter (ADC), a sampling oscillator, and a digital signal processor (DSP). The frequency switching function of the sampling oscillator is necessary to determine the analog frequency value of the sub-sampled signal. The ADC incoherently sub-samples a periodic analog signal in the absence of synchronization circuits, and the DSP performs frequency domain analysis to reconstruct the signal in the discrete time domain in the equivalent-time sense.

The proposed signal acquisition system operates under the following conditions:

- (1) the frequency of the analog signal to be acquired is assumed to be unknown, and
- (2) the sampling oscillator contains low far-out phase noise.



**Figure 17:** The proposed incoherent sub-sampling ( $f_x > f_s/2$ ) and signal reconstruction setup.

### 3.1.2 Digital Algorithms for Periodic Signal Reconstruction

#### 3.1.2.1 Discrete Frequency Estimation

Discrete frequency is the frequency measure of discrete signals determined in the range of  $[0, \pi]$  (The term is defined in Appendix B). Reconstructing the waveform from coarsely sampled data requires estimating the discrete frequency of the sampled signal as described in Section 3.1.2.2.

The discrete frequency value of a sampled signal can be found by locating a fundamental spectral peak of the discrete spectrum of the sampled signal. Such discrete spectral analysis, however, suffers from a finite spectral resolution  $\Delta_f$ , which is defined by

$$\Delta_f = \frac{\pi}{n}, \quad (21)$$

where  $n$  is the number of samples. The value of  $\Delta_f$  is hardly driven small enough since the sample size  $n$  is, in practice, limited by the available memory size of the digitizer. Any discrete frequency values can be measured only at the frequency that is an integer multiple of  $\Delta_f$ . For this reason, the discrete frequency estimation, which is

an essential procedure in the proposed signal reconstruction method, is not accurate enough without the further assistance described below.

The resolution of discrete frequency estimation can be improved if *pre-* and *post-conditioning* techniques are applied to the discrete Fourier transform (DFT) [20]. First, pre-conditioning is used to minimize the spectral leakage of the incoherently sampled signal. This signal contains a discontinuity at the beginning and the end of the sample sequence. Such a discontinuity causes spectral leakage of the discrete spectrum, as shown in Figure 18-(a), which results in reduced accuracy of the discrete frequency estimation. Signal discontinuity and spectral leakage can be minimized by multiplying the sampled signal by a window function (windowing) and then transforming it to the frequency domain using DFT. For instance, the Gaussian window, denoted by  $w$ , can be applied to the sampled signal using the normalized Gaussian function:

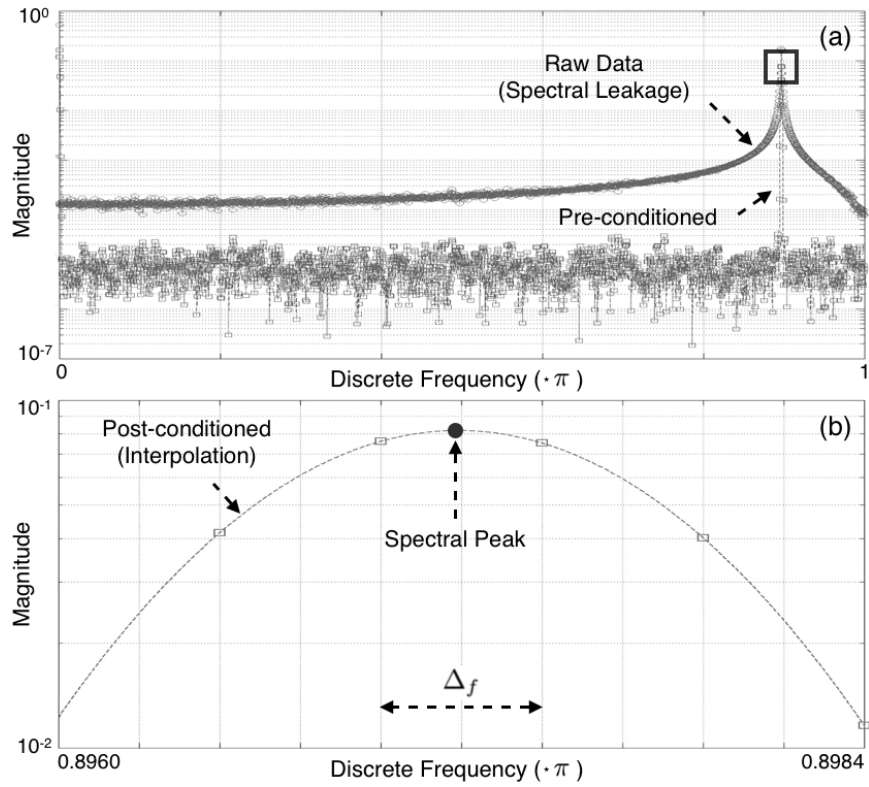
$$w[k] = e^{-(k-l/2)^2/(2\sigma^2)}, \quad (22)$$

where  $l$  denotes the window length,  $\sigma$  the standard deviation, and  $k=1, 2, \dots, l$ . The formula  $l=n$  holds true when the window is applied to the entire sampled signal. It is shown in Figure 18-(a) that the spectrum obtained from the DFT with signal pre-conditioning, denoted by  $X$ , contains less spectral leakage than the unconditioned spectrum. Second, in signal post-conditioning, the spectral points are interpolated to locate the spectral peak with enhanced resolution. In Figure 18-(b), the abscissa of the spectral maximum, which falls between the spectral bins, is located by interpolating the magnitude of three frequency bins: one with the highest magnitude and its two neighbor bins. The Gaussian interpolation method is then used to calculate the frequency estimation,  $\hat{f}_d$ , by using the following formula:

$$\hat{f}_d = \Delta_f \cdot \left( m + \frac{\ln \frac{X[m+1]}{X[m-1]}}{2 \cdot \ln \frac{X[m]^2}{X[m+1]X[m-1]}} \right), \quad (23)$$

where  $m$  denotes the index of the frequency bin with the highest magnitude.





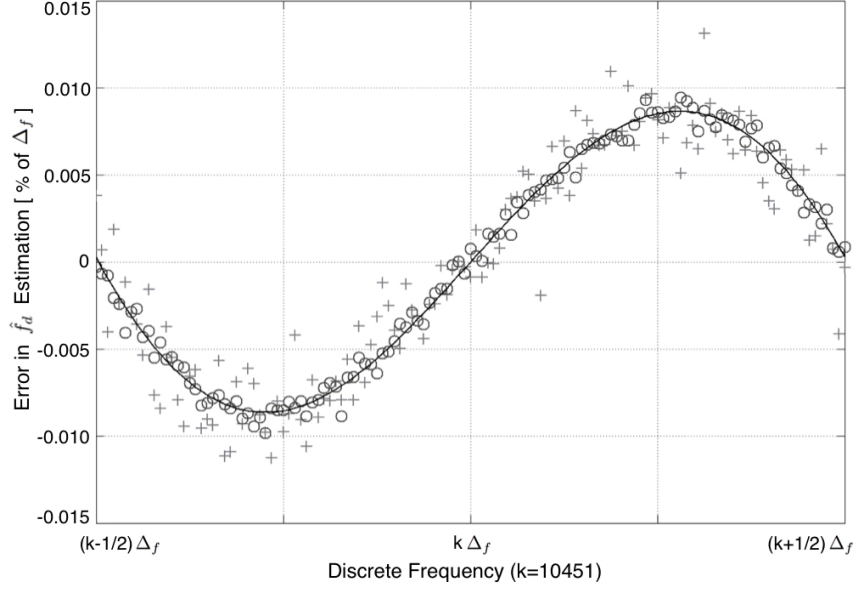
**Figure 18:** Spectral analysis for sub-sampled data: (a) with and without pre-conditioning (marked as squares and circles respectively), and (b) spectral peak estimation using post-conditioning (a magnified view of the squared region in (a)).

In computer simulation, the discrete frequency estimation accuracy obtainable from the pre- and post-conditioning was evaluated. The ADC models with sampling rate of 500 Msps, 10-, 12- and 64-bit resolution, were constructed. Note that static nonlinearity was not incorporated in these models. Analog signals (sinusoids) with various frequencies were examined to determine the discrete frequency estimation accuracy at various signal frequencies: the frequency of the analog signal was swept with the center value of  $k\Delta_f \approx 1.275756$  GHz ( $k = 10451$ ,  $\Delta_f \approx 0.1220703$  MHz), which falls exactly at the frequency bin, and with the range of  $\pm\Delta_f/2$ . For signal pre- and post-conditioning, a Gaussian window with  $r = 8$  (the ratio between the window length  $n$  and the standard deviation) and Gaussian interpolation were used, respectively. In Figure 19, the discrete frequency estimation errors are plotted for various swept signal frequencies. According to the plot, the amount of the estimation error depends on where the signal frequency resides between the DFT frequency bins. The simulation results of the highest resolution ADC show that the maximum estimation error is 0.0087% of  $\Delta_f$  at the signal frequency of  $k\Delta_f \pm 1/4\Delta_f$ . As the ADC bit resolution decreases to 12 (denoted as [o]) and 10 (denoted as [+]), the estimation errors increase but are bounded by 0.015% of  $\Delta_f$ .

### 3.1.2.2 Signal Reconstruction in the Time-Domain

In this section, the sampled signal  $x$ , sequenced according to raw sampling time as shown in Figure 16-(a), is re-mapped to represent the signal within a single fundamental cycle, as shown in Figure 16-(b). For signal re-mapping, the discrete frequency measure  $\hat{f}_d$  obtained in Section 3.1.2.1 is required to determine the discrete time of the samples. Such a discrete frequency-to-time conversion (described in Appendix B in detail) can be expressed using the modulo operation. The discrete time of the  $k$ -th sample,  $x[k]$ , is determined in the discrete time range of  $[0, 2\pi]$  by

$$t_d[k] = \text{mod}(t_d[k-1] + \hat{f}_d, 2\pi), \quad (24)$$



**Figure 19:** Discrete frequency estimation error of digitizers with bit resolution of 10 (denoted as [+]), 12 (denoted as [o]), and a value approaching machine precision (denoted as a solid line).

where  $\hat{f}_d$  is the estimated discrete frequency, and  $\text{mod}(a, b)$  is the modulo operation which finds the remainder of division of  $a$  by  $b$ . Note that this formula is the discrete version of the analog frequency-to-time conversion shown below.

$$\phi_x(t) = \phi_x(t - \Delta t) + \omega_x \cdot \Delta t, \quad (25)$$

where  $\phi_x$ ,  $\omega_x$ ,  $t$  and  $\Delta t$  denote the analog phase, angular frequency, time and time increment of a periodic signal, respectively. In the analog domain, the angular frequency defines the phase of a periodic signal at a particular time. In the discrete domain, on the other hand, the discrete frequency specifies the discrete time of a sampled signal at a particular sample point, as described in Equation 24. The only additional component in Equation 24 as compared to Equation 25 is the modular operation, which is required for the discrete time to be confined within the range of  $[0, 2\pi]$ .

Due to possible estimation error in the discrete frequency measure  $\hat{f}_d$  with respect

to the true discrete frequency value  $f_d^*$ , the discrete time of the sampled signal can be determined incorrectly: the error in  $t_d[k]$  accumulates over  $k$  ( $= 1, 2, \dots, n$ ). Thus, a small error  $\epsilon_{f_d}$  in the estimated discrete frequency can result in large discrete time errors for large values of  $k$

$$\epsilon_{t_d}[k] = \text{mod}(k \cdot \epsilon_{f_d}, 2\pi), \quad (26)$$

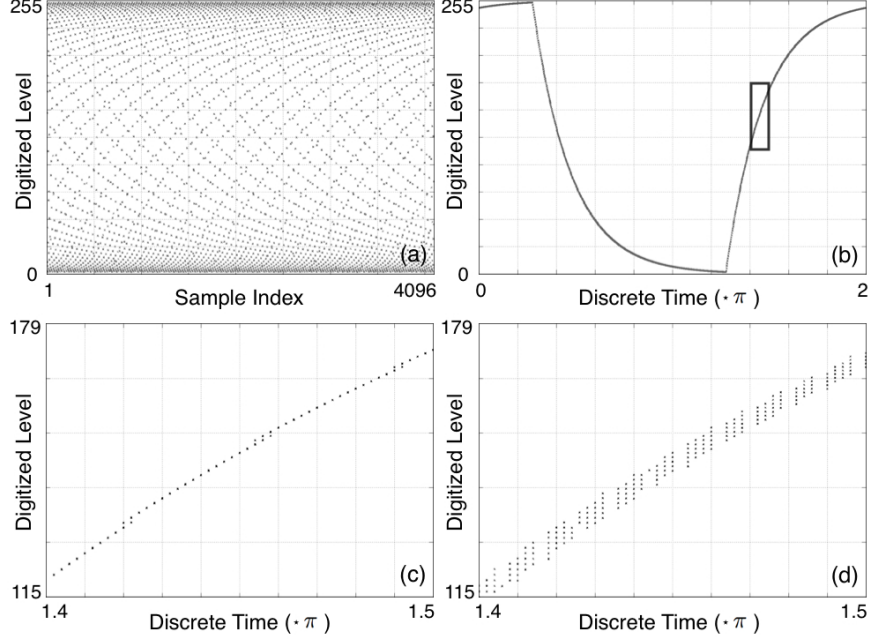
$$\epsilon_{f_d} = \left| \hat{f}_d - f_d^* \right|. \quad (27)$$

According to the equations above, the discrete frequency estimation error should be lower than 1% of  $\Delta_f$  to bound the discrete time error to 0.01.

The proposed phase re-mapping method was simulated using a 10-bit ADC without additional amplitude and timing noise. An analog signal (square wave) was acquired at the sampling rate of 1.159 times the analog signal frequency. The discrete frequency of the sampled signal was located with an estimation error of 0.0097% of  $\Delta_f$ . Using the discrete frequency measure, the sub-sampled signal was reconstructed into a single cycle of the waveform. The sub-sampled raw data and the reconstructed signal are shown in Figure 20-(a) and -(b), respectively. Figure 20-(c) is a magnified view of the squared area in Figure 20-(b). To show how the discrete frequency estimation error distorts the reconstructed signal, the error of 1% of  $\Delta_f$  was intentionally applied to  $\hat{f}_d$ . The waveform reconstructed from the erratic frequency measure is plotted in Figure 20-(d), which shows discrete time dispersion of  $\approx 0.01\pi$  (peak-to-peak value).

### 3.1.2.3 Jitter-Induced Noise Suppression

In case a sampling oscillator is unstable and generates a signal with timing noise (or jitter), the sampled signal obtained from this unstable time-base contains jitter-induced sampling noise. The waveform that is reconstructed from such a noisy sampled signal also involves discrete time noise in the discrete time domain. This type



**Figure 20:** Reconstruction of sub-sampled clock signal: (a) data in a raw sequence, (b) the reconstructed waveform, (c) the magnified view of the squared region in (b), and (d) the reconstructed waveform resulted from an erratic frequency estimation.

of noise in the reconstructed waveform is represented as a time-dispersed waveform in the discrete time domain.

To compensate the reconstructed waveform for jitter-induced sampling noise, a discrete frequency tracking method is used. Timing jitter of an unstable oscillator can be seen as unstable (or time-varying) operation frequency in the frequency domain [3]. For this reason, the time-varying frequency information of the sampling oscillator is used for jitter tracking (or compensation), instead of using the constant (or averaged) frequency value as shown in Equation 24. In addition, the time-varying frequency information does not need to be measured directly from the sampling oscillator, rather observed indirectly from time-varying components in the discrete spectra of the sampled signal. Note that the time-varying (discrete) frequency tracking method only suppresses long-term jitter components since it does not track short-term fluctuations in sampling frequency.

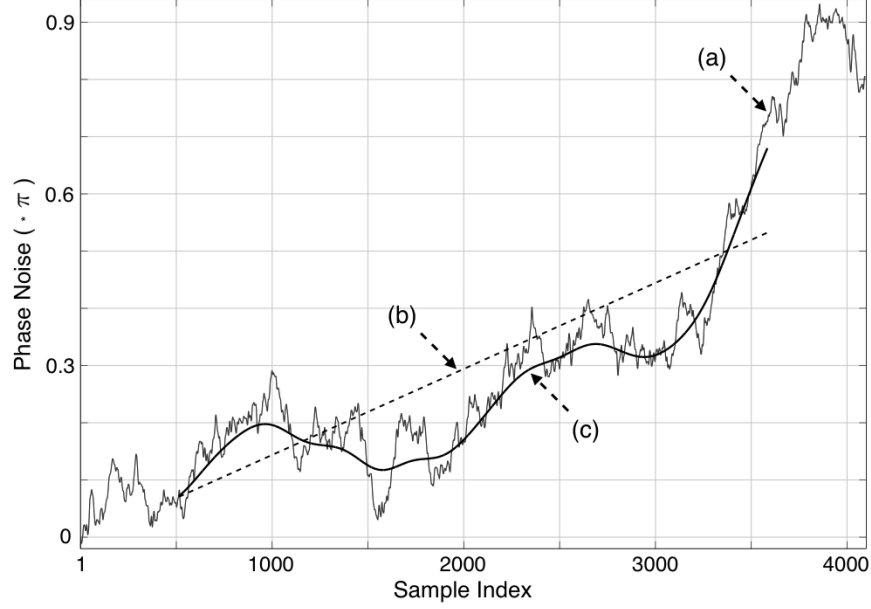
Time-varying discrete frequency can be detected by using the short-time Fourier

transform (STFT) of the sampled signal, where each of the time-windowed signal spectrum represents the frequency components within the time period of the time-windowed signal. The estimated discrete frequency value (from the STFT results) as a function of the sample index  $k$ ,  $\hat{f}_d[k]$ , is used for the discrete frequency-to-time conversion (the modification of Equation 24):

$$t_d[k] = \text{mod}(t_d[k-1] + \hat{f}_d[k], 2\pi). \quad (28)$$

Since  $\hat{f}_d[k]$  tracks the frequency fluctuation of the sampling oscillator over time, Equation 28 results in the discrete time value of  $t_d[k]$  that compensates for jitter of the unstable sampling oscillator. Thus, the reconstructed signal based on  $t_d[k]$  contains less dispersion in the discrete time domain. In fact, the jitter compensation bandwidth is determined by the discrete frequency detection bandwidth of the STFT-based spectral analysis.

The proposed noise suppression technique was evaluated using computer simulation. A harmonically related multi-tone signal (the fundamental of  $\approx 3.853$  GHz and its third and fifth order harmonics) were generated and digitized (assuming no quantization errors). First, the sampled signal was reconstructed into the  $[0, 2\pi]$  discrete time range with and without the jitter-induced noise suppression. The performance of the noise suppression was evaluated by comparing the noise-suppressed result to the one without noise-suppression. On the merit of simulation, the discrete time dispersion of the reconstructed waveforms can be quantized directly from the plot of the sample index versus phase (time) error as shown in Figure 21. The phase noise applied to the 1 GHz sampling oscillator is denoted by (a). The phase estimation (b) is based on Equation 24 (the constant discrete frequency estimation), and the phase estimation (c) is from Equation 28 (the time-varying discrete frequency estimation). The time-varying discrete frequency value used to generate the plot (c) is derived by using the time window width of 1024 samples and shown in Figure 22. The reconstructed waveforms based on (b) and (c) are shown in Figure 23(a) and Figure

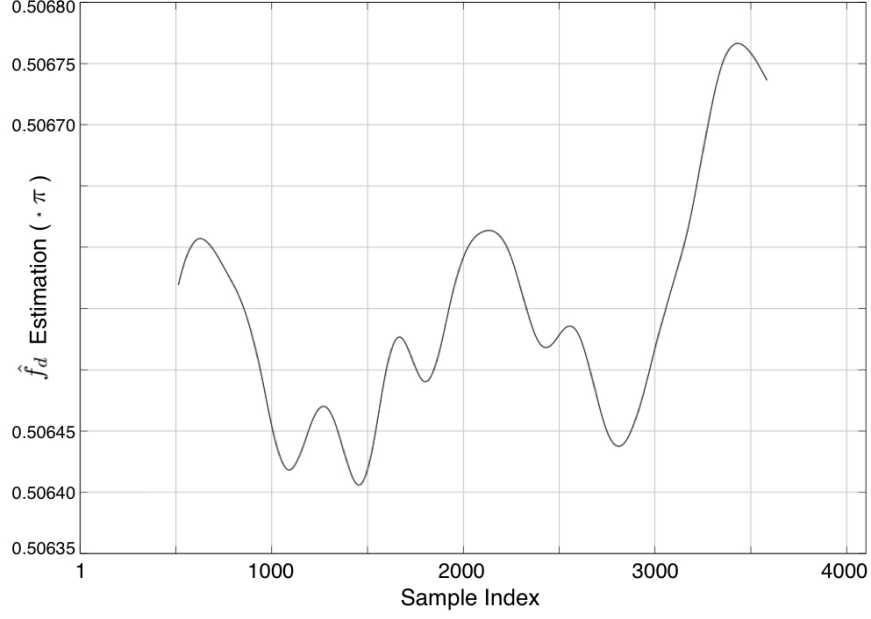


**Figure 21:** Phase noise estimation: (a) the instantaneous phase noise of a sampling oscillator, (b) the phase noise estimation based on the constant discrete frequency measure, and (c) the phase noise estimation using the STFT-based time-varying discrete frequency detection.

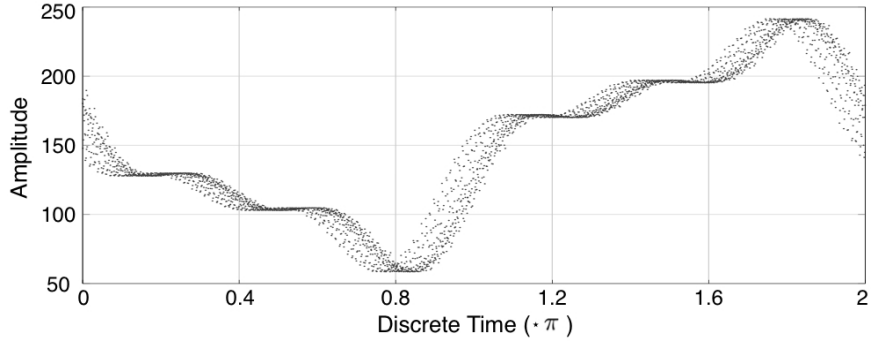
23(b) respectively. The amounts of discrete time dispersion in the two waveforms were calculated from the data in Figure 21. The reconstructed signal without the noise suppression in Figure 23(a) contains the discrete time dispersion of  $\approx 0.12067$  rms, and the one with the noise suppression in Figure 23(b) contains the discrete time dispersion of  $\approx 0.027786$  rms.

### 3.1.3 Analog Frequency Recovery

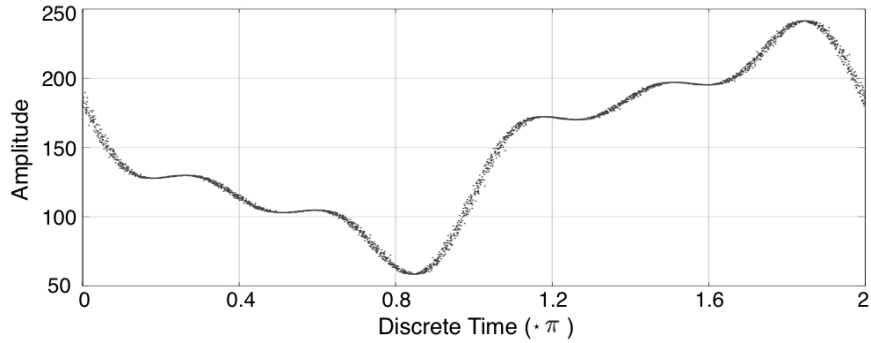
Conventional sub-sampling architectures are not able to extract analog frequency information from digitized signals because of spectrum aliasing distortion [61]. Only the discrete frequency is retained in discrete signals. On the contrary, to enable a digitizer to specify the analog frequency of sampled signals, the proposed technique utilizes a sampling rate switch. As the sampling speed deviates by a small amount (digitally controlled in hardware), the analog frequency of the sampled signal can be located by observing the vector of discrete line spectra movement. In the case that



**Figure 22:** STFT-based time-varying discrete frequency estimation.



(a) A simulation result of the reconstruction of a multi-tone signal without jitter-induced noise suppression.



(b) A phase-noise suppressed form of Figure 23(a) using the time-varying discrete frequency estimation and jitter-induced noise suppression technique.

**Figure 23:** Comparison of the signal reconstruction with and without jitter-induced noise suppression.



analog frequency value  $f_x$  resides in the  $k$ -th Nyquist range

$$(k-1) \cdot \frac{f_s}{2} < f_x < k \cdot \frac{f_s}{2}, \quad (29)$$

where  $k$  is a positive integer and  $f_s$  is the sampling frequency, the spectral peak in the discrete spectrum is located at

$$\hat{f}_d = |f_x - \lfloor \frac{k}{2} \rfloor f_s| \cdot \frac{\pi}{f_s/2}, \quad (30)$$

by definition of discrete frequency described in Appendix B. The absolute value operator,  $|f_x - \lfloor \frac{k}{2} \rfloor f_s|$ , is introduced to address a folding effect which occurs when a sampled signal is aliased in the discrete frequency domain, and the term,  $\frac{\pi}{f_s/2}$ , is a normalization factor for the discrete frequency range  $[0, \pi]$ . If the sampling speed of the digitizer is switched from  $f_s$  to  $f_s + \Delta f_s$ , the spectral peak is re-located to

$$\hat{f}_d + \Delta \hat{f}_d = |f_x - \lfloor \frac{k}{2} \rfloor (f_s + \Delta f_s)| \cdot \frac{\pi}{(f_s + \Delta f_s)/2}. \quad (31)$$

Subtracting Equation 30 from Equation 31, the amount of discrete frequency shift is determined as

$$\Delta \hat{f}_d = \begin{cases} -f_x \cdot \frac{2\Delta f_s}{f_s(f_s + \Delta f_s)} \cdot \pi & k = \text{odd} \\ +f_x \cdot \frac{2\Delta f_s}{f_s(f_s + \Delta f_s)} \cdot \pi & k = \text{even} \end{cases}. \quad (32)$$

Solving for  $f_x$  using Equation 32, the analog frequency value  $f_x$  is *preliminarily* determined as,

$$f_x = \left| \frac{\Delta \hat{f}_d}{\pi} \right| \cdot \frac{f_s(f_s + \Delta f_s)}{2\Delta f_s}. \quad (33)$$

Note that  $\Delta \hat{f}_d$  and  $\Delta f_s$  are possibly incorrect due to limited measurement accuracies. The analog frequency value  $f_x$  obtained in Equation 33 is used only for determining the Nyquist range index  $k$ . Resolving for  $f_x$  using Equation 30,  $f_x$  is determined using  $k$ , the Nyquist range index determined using Equation 29.

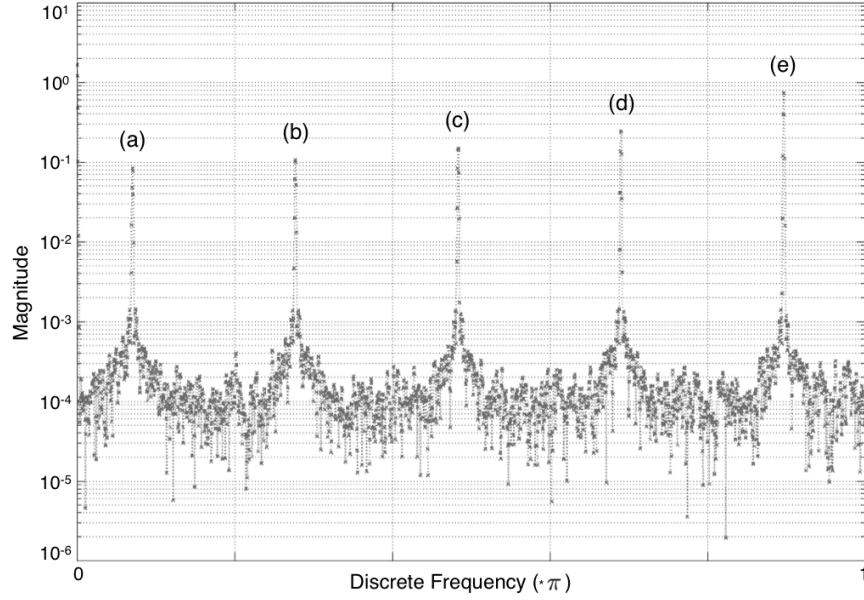
$$f_x = \begin{cases} \lfloor \frac{k}{2} \rfloor f_s + \frac{\hat{f}_d f_s}{2\pi} & k = \text{odd} \\ \lfloor \frac{k}{2} \rfloor f_s - \frac{\hat{f}_d f_s}{2\pi} & k = \text{even} \end{cases}, \quad (34)$$

assuming the sampling frequency  $f_s$  is known accurately.

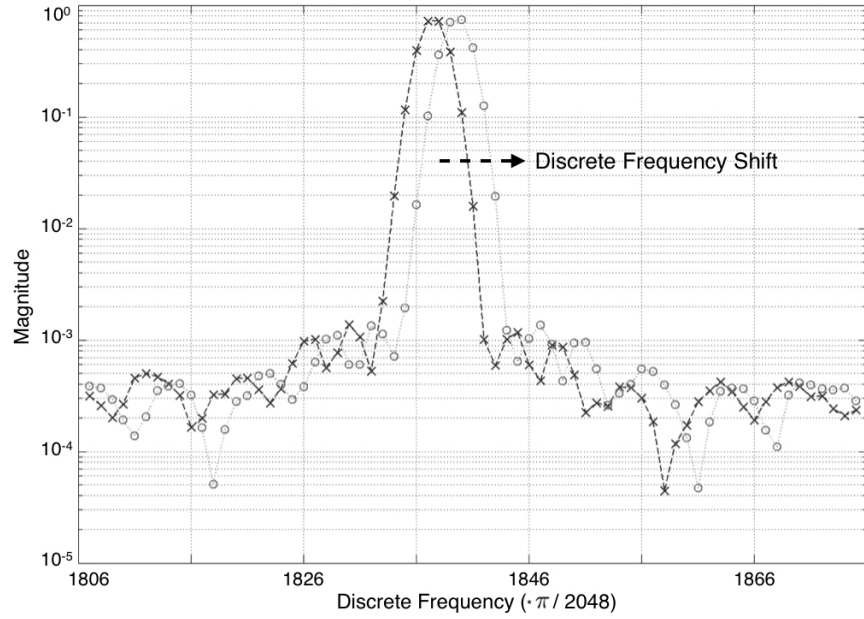
The amount of the discrete frequency shift,  $\Delta\hat{f}_d$ , due to the digitizer sampling frequency switching is, in general, smaller than DFT frequency resolution. However, the value of  $\Delta\hat{f}_d$  is still resolvable if signal pre- and post-conditioning described in Section 3.1.2.1 are used to enhance DFT resolution. To determine the feasibility of the analog frequency recovery, a computer simulation was performed. In the simulation, a noisy multi-tone signal ( $\approx 1.276$ -GHz square wave which consists of up to the ninth harmonic of the fundamental tone, which shows an SNR of 95.91 dB) was incoherently sub-sampled at the sampling speed of 500 Msps. In Figure 24, the spectra of the multi-tone signal (before applying the sampling frequency switching) are shown. First, the analog frequency cannot be extracted due to spectrum aliasing. Second, the fundamental tone, which is noted as (e) in Figure 24, can be identified only under the assumption that the fundamental frequency contains the highest power. To resolve these limitations, the same multi-tone signal was re-sampled at the sampling speed of 500.1 Msps. Then, spectral locations of two sampling results are compared to each other for specifying  $\Delta\hat{f}_d$ . The discrete frequency shift of the spectrum (e) due to the sampling frequency switching is shown in Figure 25. The obtained simulation results are summarized in Table 1: The spectrum (e) represents the fundamental tone (1.276 GHz) of the sampled multi-tone signal, and the spectra (d), (c), (b) and (a) are the 3rd, 5th, 7th and 9th harmonics respectively.

**Table 1:** Sampling Frequency Switching Results

Tone	$\Delta f_s$ (kHz)	$\hat{f}_d (\cdot\pi)$	$\Delta\hat{f}_d (\cdot\pi)$	$k$	$f_x$ (GHz)
(a)	100	0.070992	0.009183	46	11.482
(b)	100	0.277546	0.007143	36	8.931
(c)	100	0.484101	0.005101	26	6.379
(d)	100	0.690656	0.003061	16	3.828
(e)	100	0.897211	0.001020	6	1.276



**Figure 24:** The spectra of the multi-tone periodic signal (sub-sampled at 500 Msps).

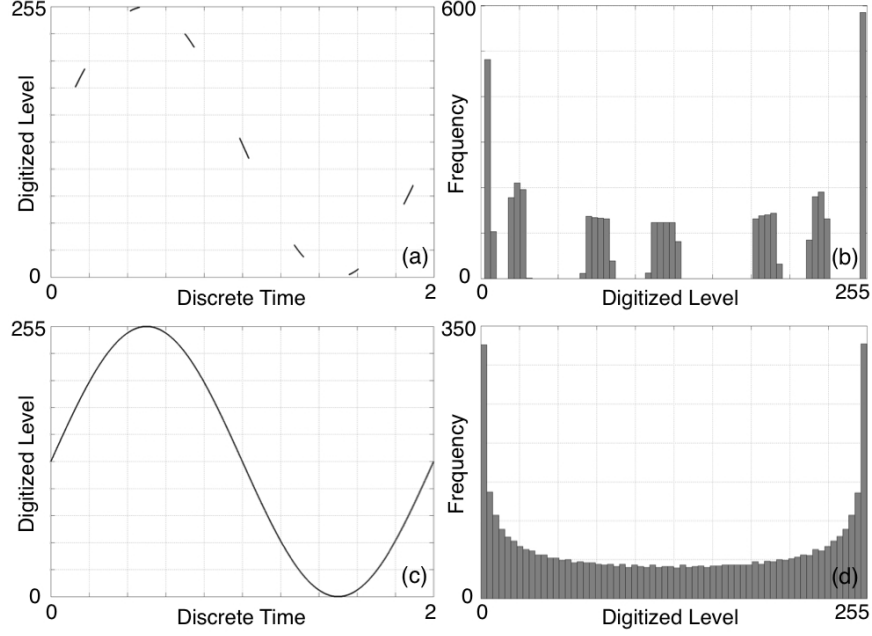


**Figure 25:** The sampling speed switching differentiates the discrete frequency of the sampled signal-(e): (x) at sampling speed of 500 Msps, and (o) at sampling speed of 500.1 Msps.

### 3.1.4 Problematic Sample Distribution

In some problematic sampling cases, a reconstructed signal contains samples that are stuck together in the discrete time domain. Under such conditions, the discrete time values of multiple samples are identical, and those samples locate at the same position in discrete time. Consider, for instance, a coherent sub-sampling case in which two entire cycles of a periodic signal are sampled at eight points in time. The discrete time values of the samples are consecutively  $0, (1/2)\pi, \pi, (3/2)\pi, 0, (1/2)\pi, \pi, (3/2)\pi$ . The first four samples form one cycle of the signal, and the other four samples construct another cycle of the signal, which is identical to the previous one. Some samples are stuck to the others, and the information contents of the samples are duplicated. For this reason, the effective sampling rate is reduced to twice the Nyquist rate. To prevent this, the number of cycles of the signal to be sampled can be changed (three cycles of the signal are sampled at eight points in time). The resulting samples are not stuck (or close) to each other. Such a solution to problematic coherent sampling is generalized and shown in Appendix C. In contrast, perfect duplication of sample contents may not occur in incoherent sub-sampling, but the effective sampling rate can be compromised for a similar reason. Consider an incoherent sub-sampling case in which 2.01 cycles of a periodic signal are sampled at eight points in time. This incoherent sub-sampling case is very similar to the previous problematic coherent sub-sampling case. The samples are not perfectly stuck together, but located very close to each other. Since the samples are not equally distributed over the signal, the effective sampling rate of the digitizer is compromised. As a solution to this problematic incoherent sub-sampling case, the sampling speed can be adjusted and the number of cycles to be sampled is different from that of any problematic coherent sub-sampling cases. See Appendix C for a generalized formulation.

A reconstructed signal with stuck samples is shown in Figure 26(a) using computer simulation. The corresponding sample distribution contains null bins as shown in

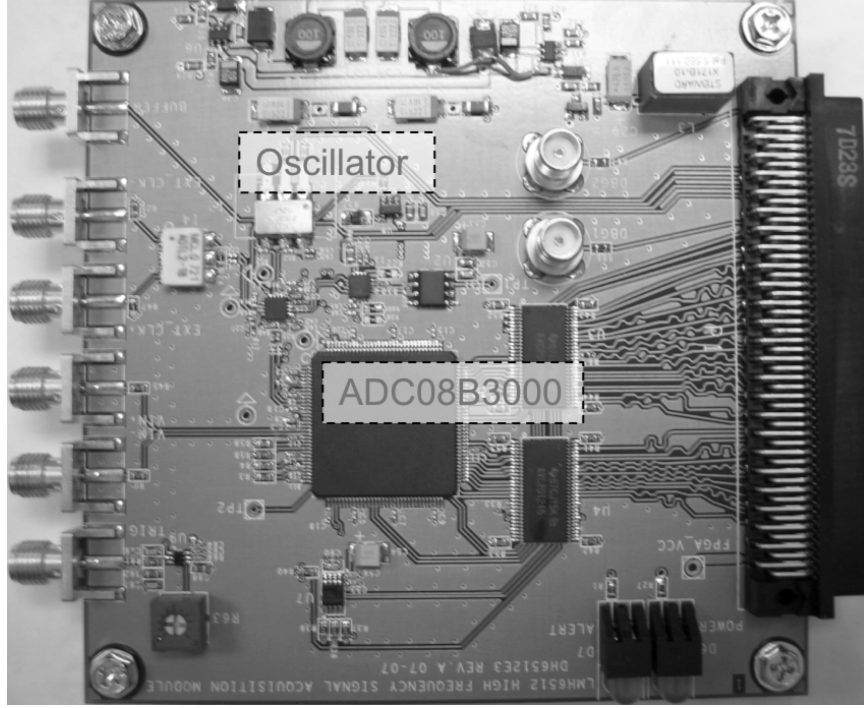


**Figure 26:** Distribution of the digitized samples: (a) a localized reconstructed signal, (b) the histogram obtained from (a), (c) an unlocked reconstructed signal, and (d) the histogram obtained from (c)

Figure 26(b). To release the stuck samples, a small offset frequency was injected to the sampling frequency, and the analog signal was re-sampled. The re-sampled signal is distributed over the entire dynamic range of the signal as shown in Figure 26(c) and shows an unlocalized distribution as shown in Figure 26(d). Note that, in hardware experiments, the sampling frequency control is enabled by a frequency controllable sampling oscillator (a voltage-controlled surface acoustic wave (SAW) oscillator with a digital frequency control is used in Section 3.2).

### 3.2 Validation

The proposed incoherent sub-sampling architecture was implemented on a printed circuit board (PCB) utilizing a digitizer (National Semiconductor ADC08B3000) with 8-bit resolution, 3-GHz bandwidth, 4-kByte built-in memory as shown in Figure 11. The sampling clock for the digitizer was provided by a surface acoustic wave (SAW) based voltage-controlled oscillator (Crystek CVS575), whose nominal frequency was 719



**Figure 27:** Picture of the incoherent sub-sampling digitizer with the interface to an FPGA.

MHz. This oscillator was equipped with a digital control to its operation frequency. In addition, the signal reconstruction was performed using a field programmable gate array (FPGA) (XC3S200 Spartan3) on a separate PCB.

### 3.2.1 Discrete Frequency Estimation

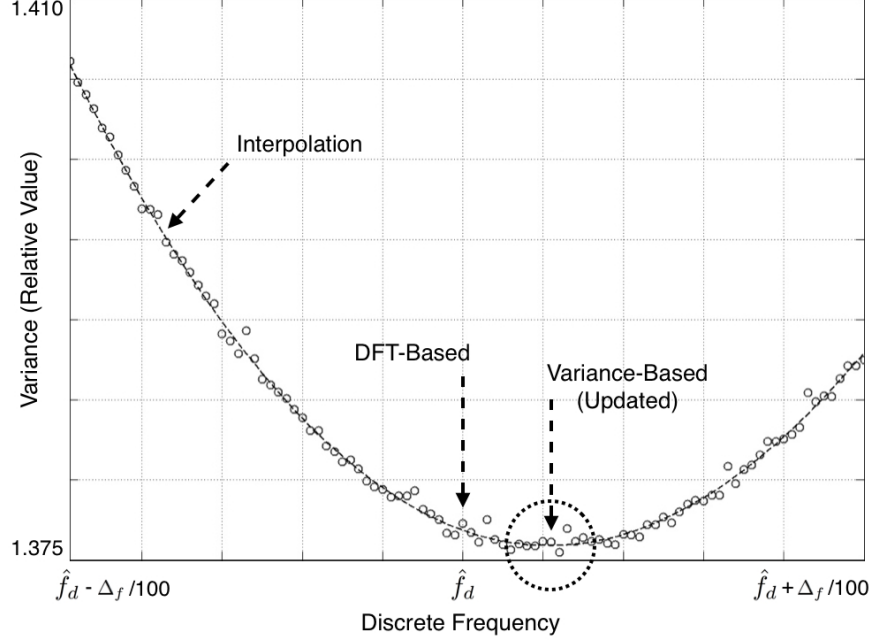
When the discrete frequency estimation is evaluated with hardware, it may be less accurate than that performed through software simulation due to the non-idealities of hardware. In this subsection, first, the accuracy of the discrete frequency measurement, which is described in Section 3.1.2.1, is verified in hardware. Second, a fine tuning of the obtained discrete frequency value  $f_d$  is performed to obtain a more accurate value of  $f_d$ . In this fine tuning, the discrete frequency deviation (up to 1% of  $\Delta_f$ ) is added to the initially estimated value of  $f_d$ , and the deviated frequency value is re-applied to the discrete frequency-to-time conversion as shown in Equation 24. The sampled signal is iteratively reconstructed based on each deviated value of  $f_d$ . Based

on the iterative method, the value of more accurate measures of  $f_d$  can be obtained by searching for the best reconstructed signal (the one with the least discrete time dispersion).

For experimental purposes, a 1.5-GHz sinusoidal waveform was generated from a signal generator (Agilent E4437B) and fed to the signal acquisition board. The discrete frequency of the sampled signal was calculated in the FPGA using the pre- and post-conditioning technique described in Section 3.1.2.1 and denoted as  $\hat{f}_d$  in Figure 28. Frequency measurement accuracy was evaluated by computing the discrete time dispersion of the reconstructed signal (based on  $\hat{f}_d$ ) and denoting this by the label *DFT-based* in Figure 28. The deviation of up to  $\pm 1\%$  of  $\Delta_f$  is then applied to the initially obtained discrete frequency  $\hat{f}_d$ , and the sampled signal is iteratively reconstructed. The discrete time variance values of each reconstructed signal are plotted. The lowest discrete time variance (phase dispersion) should correspond to the exact measurement of the discrete frequency. The estimated discrete frequency value after the fine tuning (denoted by the label *variance-based*) shows an estimation error of  $\approx (-)0.2\%$  of  $\Delta_f$  in this particular experimental setup.

### 3.2.2 Jitter-Induced Noise Suppression

The performance of the jitter-induced noise suppression technique described in Section 3.1.2.3 was evaluated by incoherently sub-sampling a 1-GHz digital clock signal generated by an Agilent 8133A signal generator. Figure 29(a) shows the reconstructed signal based on the constant discrete frequency value. Any dispersion of the reconstructed signal in the discrete time domain is due to sampling time errors, assuming the sampled analog signal is clean. The time-varying discrete frequency value was used to revise the signal reconstruction, as shown in Figure 29(b). This noise-suppressed reconstructed waveform contained less phase spread compared to the waveform in



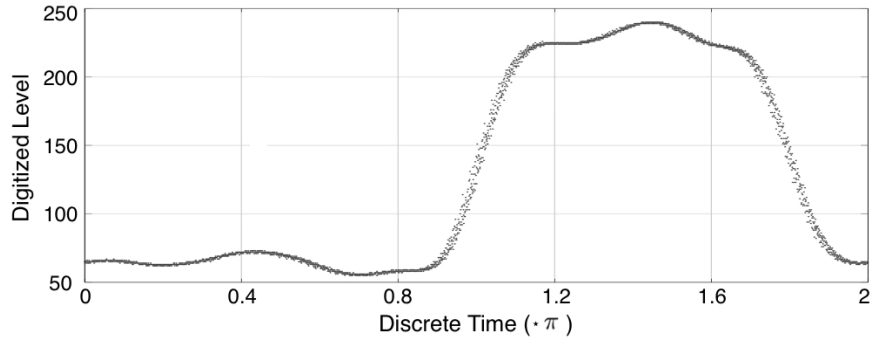
**Figure 28:** Discrete frequency estimation by searching for the reconstructed signal with the least time variance.

Figure 29(a). Quantizing the amounts of phase dispersion of the waveforms in Figure 29(a) and 29(b) requires a virtual clean reference waveform. Such a reference waveform was obtained by regressing the waveform in Figure 29(b). The discrete time dispersion of the reconstructed signal was calculated by comparing the signal to the reference waveform. Figure 29(c) shows the dispersion of the waveform in Figure 29(a) with histogram, which indicates a standard deviation of  $\approx 0.0031472$ , and Figure 29(d), which is calculated from the waveform in Figure 29(b), represents the standard deviation of  $\approx 0.0014099$ .

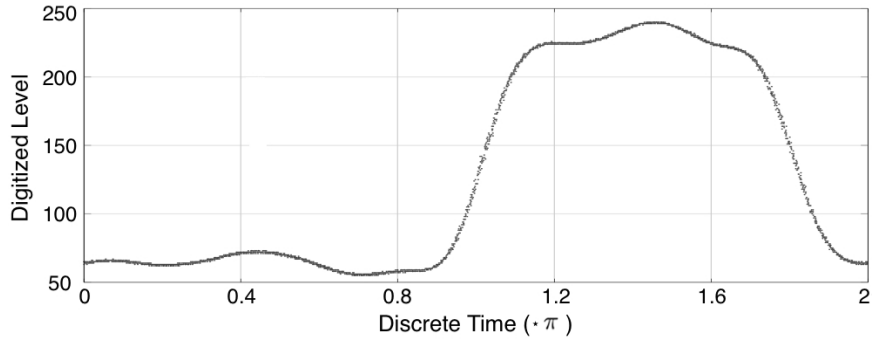
### 3.2.3 Comparison with Standard Instrumentation

The performance of the proposed signal acquisition technique was compared with that of the other standard instrument by digitizing a high-frequency analog signal (pulse) using both the proposed signal acquisition board and a commercial digital oscilloscope (WavePro 7000A, 20-Gsps effective sampling rate, 3-GHz bandwidth) following the experimental setup shown in Figure 30. Through the path (a) noted

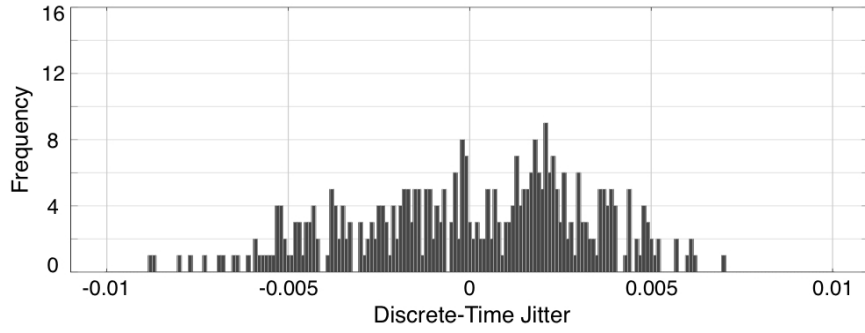




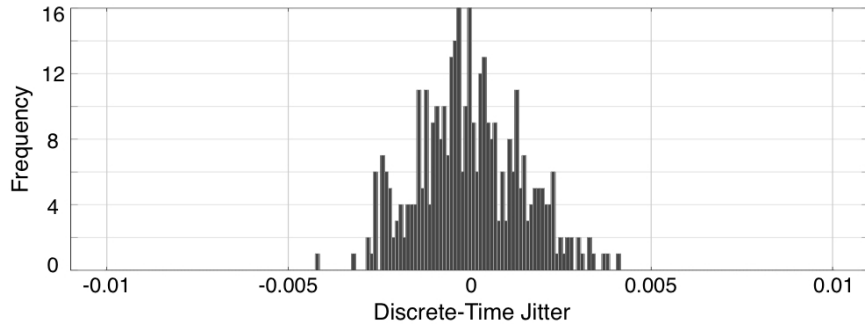
(a) A reconstructed signal without jitter-induced noise suppression.



(b) A reconstructed signal with jitter-induced noise suppression.

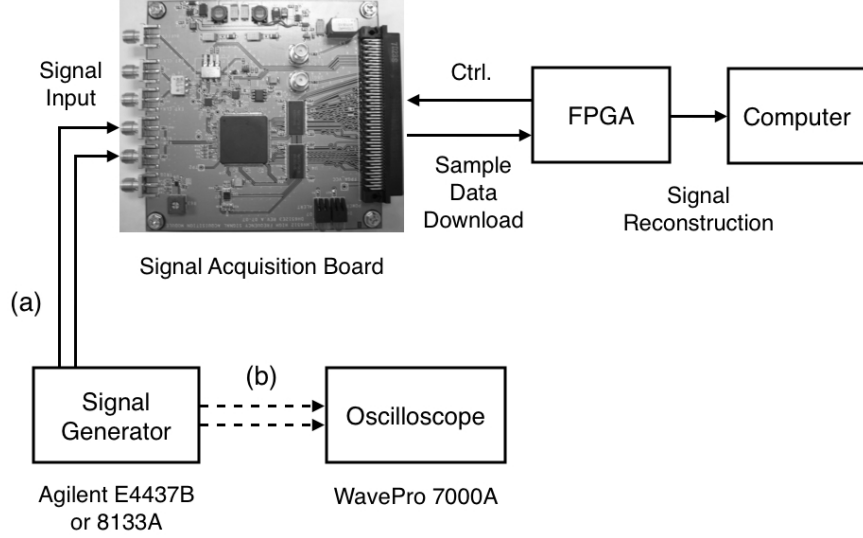


(c) Discrete time error (dispersion) histogram of the signal shown in 29(a).



(d) Discrete time error (dispersion) histogram of the signal shown in 29(b).

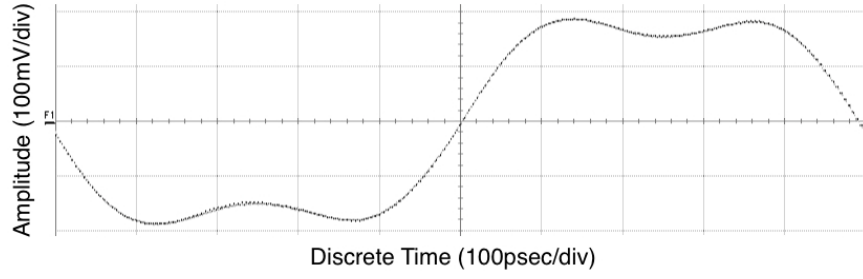
**Figure 29:** Hardware experiment of jitter-induced noise suppression.



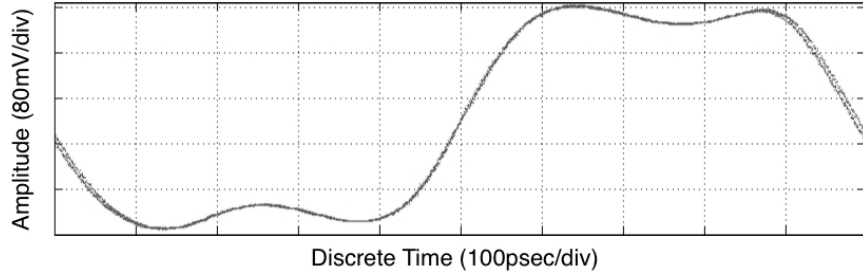
**Figure 30:** A hardware experiment setup for signal acquisition using both (a) the DSP-based incoherent undersampling technique and (b) a commercial digital oscilloscope.

in the figure, differential analog signals were digitized (sub-sampled) by the signal acquisition board, and the discrete frequency estimation and signal reconstruction were performed in the following FPGA and computers. The analog frequency of the digitized signals was recovered by switching the sampling speed to a slightly different frequency ( $\Delta f_s \approx 1.305$  MHz) using the digital control on the FPGA board.

The sampling results of 1-GHz, 2-GHz and 3-GHz pulse signals using the proposed signal acquisition method are compared with signal acquisitions from a commercial oscilloscope (WavePro 7000A) in Figures 31, 32 and 33, respectively. Notice that displayed waveforms from the WavePro 7000A are the averaged values, which do not represent a dispersion due to sampling time inaccuracy. In comparison, the waveforms obtained from the proposed method contain 4096 samples without averaging. In addition, the calculated rise/fall time, peak-to-peak voltage and slew rate are summarized in Table 2.

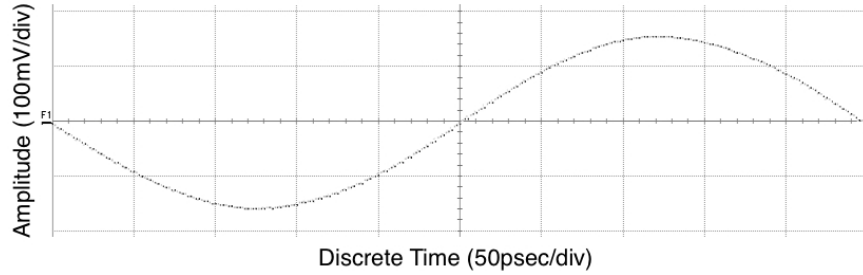


(a) A 1-GHz reconstructed clock signal obtained from WavePro 7000A (averaging mode).

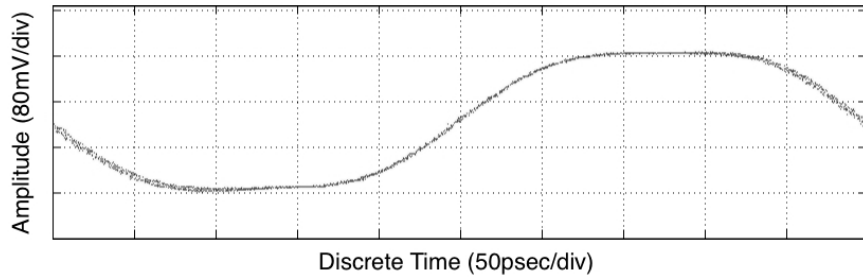


(b) A 1-GHz reconstructed clock signal obtained from the proposed method.

**Figure 31:** Performance comparison of the proposed signal acquisition with standard instrumentation (1-GHz clock signal acquisition).

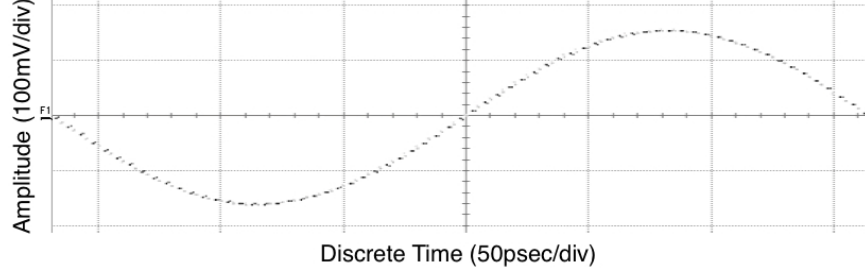


(a) A 2-GHz reconstructed clock signal obtained from WavePro 7000A (averaging mode).

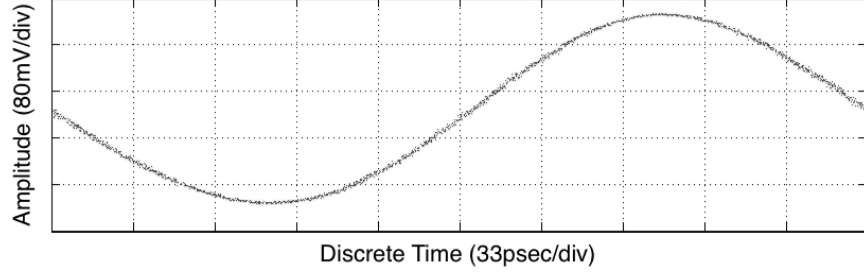


(b) A 2-GHz reconstructed clock signal obtained from the proposed method.

**Figure 32:** Performance comparison of the proposed signal acquisition with standard instrumentation (2-GHz clock signal acquisition).



(a) A 3-GHz reconstructed clock signal obtained from WavePro 7000A (averaging mode).



(b) A 3-GHz reconstructed clock signal obtained from the proposed method.

**Figure 33:** Performance comparison of the proposed signal acquisition with standard instrumentation (3-GHz clock signal acquisition).

### 3.2.4 Jitter Requirements for Sampling Time-Base Signals

A high-speed ADC demands a low-jitter sampling clock to preserve signal-to-noise ratio (SNR). In particular, the best case noise floor of the digitizer (National Semiconductor ADC08B3000), which is used for the hardware experiment in Section 3.2, is -49.9 dBc/Hz. From this level, the noise floor increases further due to noise factors such as sampling clock jitter, intrinsic ADC aperture jitter, ADC nonlinearity, and thermal noise voltage. If only aperture jitter and sampling clock jitter are considered (assuming the other noise factors are negligible), total SNR can be derived from these jitter values and the analog signal frequency  $f_x$  [13]. According to manufacturer datasheets for the digitizer and the sampling oscillator (Crystek CVS575), which are used for the hardware experiment, the aperture jitter and the sampling clock jitter are specified as 400 fs rms and 200 fs rms (max, 0.05-80 MHz) respectively. The achievable total SNR is calculated for various frequencies of the analog signal to be

**Table 2:** Signal Measurement from Digitized Samples shown in Figure 31, 32 and 33.

Case	Risetime (ps)	Falltime (ps)	Pk-Pk (mV)	Slew Rate (V/ns)
Figure 31(a)	135	129	376	2.228
Figure 31(b)	145	148	403	2.333
Figure 32(a)	120	125	316	2.207
Figure 32(b)	95	102	250	2.305
Figure 33(a)	101	100	319	2.527
Figure 33(b)	94	105	333	2.834

sampled as shown in Table 3.

**Table 3:** Achievable SNR (For Various Analog Frequency  $f_x$ )

$f_x$ (GHz)	SNR (dB)	$f_x$ (GHz)	SNR (dB)
0.5	49.1	3.0	40.9
1.0	47.4	3.4	39.7
1.5	45.5	4.0	38.6
2.0	43.8	4.5	37.7
2.5	42.2	5.0	36.8

In addition, the far-out jitter (phase noise) of the sampling clock oscillator is critical because the signal acquisition time of the proposed technique is relatively short; it takes  $2.848 \mu\text{s}$  to collect 4096 samples for 1.438 Gsps sampling speed. The incorporated sampling oscillator presents phase noise of -138.11 dBc/Hz and -137.72 dBc/Hz at the offset of 100 kHz and 1 MHz, respectively.

### 3.3 Summary

This chapter presents a high-speed periodic signal acquisition technique using incoherent sub-sampling and back-end signal reconstruction algorithms. The signal reconstruction algorithms employ a frequency domain analysis for frequency estimation and suppression of jitter-induced sampling noise. If the sampling rate of a digitizer is switched, the analog frequency value of the sampled signal can be recovered. The hardware validation indicates that the proposed signal reconstruction algorithms are able to reconstruct multi-tone high-speed periodic signals in the discrete time domain.

The new signal acquisition technique simplifies signal acquisition hardware for testing and characterization of high-speed analog and digital signals.

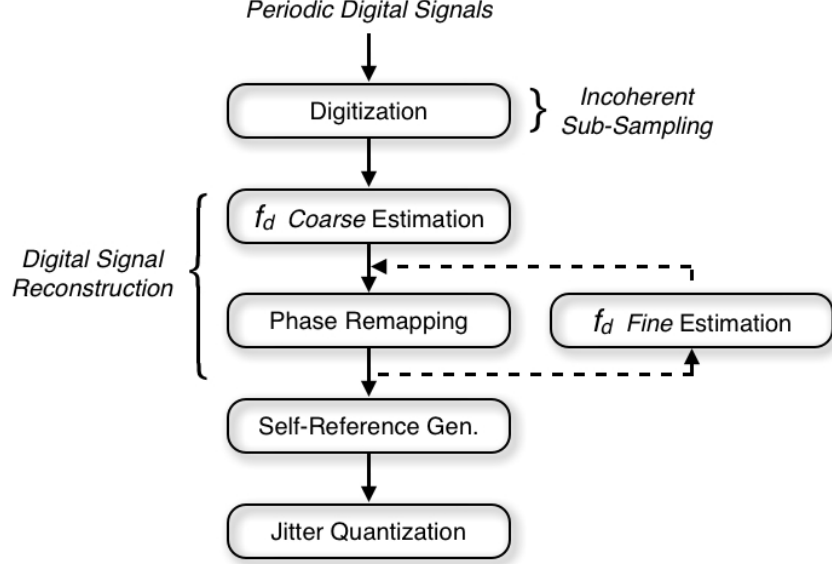
## CHAPTER IV

# SOFTWARE CLOCK RECOVERY AND JITTER QUANTIZATION IN THE RECONSTRUCTED DISCRETE-TIME DOMAIN

### 4.1 Software Clock Recovery Algorithms for PRBS Reconstruction

In this section, new digital signal reconstruction algorithms are introduced to reconstruct an incoherently sub-sampled pseudo-random bit sequence (PRBS) into a single period of the waveform (in the discrete-time domain). When the pattern length of the PRBS is  $l$ , the PRBS is deterministic (or periodic) and repeats the same pattern every  $l$  bits. Due to the periodicity, the discrete fundamental frequency  $f_d$  of the sub-sampled PRBS can be identified from its frequency spectrum. The  $f_d$  identification (or estimation) procedure consists of two parts:  $f_d$  *coarse* estimation and  $f_d$  *fine* estimation. In the  $f_d$  coarse estimation, the value of  $f_d$  is estimated by locating a spectral peak in the DFT-based discrete spectrum. The obtained discrete frequency value is used for *time re-mapping* the samples of the sub-sampled PRBS. Then, to further enhance the  $f_d$  estimation accuracy, the spectrum-sparsity based  $f_d$  estimation is iteratively performed as the fine  $f_d$  estimation. The flow chart of these algorithms is shown in Figure 34.

To provide background information for the signal reconstruction algorithms to be detailed in the following sub-section, the discrete spectrum of an incoherently sub-sampled PRBS is derived using computer simulation. The  $l$ -bit continuous-time PRBS is shown in Figure 35(a), and its autocorrelation function representing a triangle train is shown in Figure 35(b) [51]. Then, the discrete Fourier transform of the



**Figure 34:** Block diagram of the proposed jitter characterization method.

autocorrelation function, also called power spectral density (PSD), containing multiple and complex spectral peaks (whose magnitude is limited by the  $\text{sinc}^2$  envelope function) is shown in Figure 35(c). In comparison with the continuous-time signal described above, the discrete spectrum of the (incoherently) sub-sampled PRBS suffers from signal aliasing, making the resultant spectrum even more complex. An example of the PSD of the incoherently sub-sampled PRBS is shown in Figure 35(d), in which the fundamental discrete frequency component to be identified is denoted by  $f_d$ .

#### 4.1.1 Discrete Frequency Coarse Estimation

In the  $f_d$  coarse estimation, the discrete fundamental frequency  $f_d$  of the incoherently sub-sampled PRBS is identified by locating the (fundamental) spectral peak in the DFT-based discrete spectrum. However challenging it is due to the complex and rich spectrum of the sub-sampled PRBS.

First, the PRBS is a digital signal with a complex bit pattern and contains multiple spectral peaks in the frequency domain. Sub-sampling the PRBS introduces signal aliasing to the discrete-time PRBS and the resultant discrete spectrum of the PRBS



is even more complex. For this reason, the fundamental tone of the discrete spectrum is not simply the one with the lowest discrete-frequency. Some aliased spectral components may appear before the fundamental tone. To locate the spectral peak contributed by the fundamental frequency component (out of many others), the one of the lowest discrete frequency among those whose magnitude is above the threshold magnitude needs to be found as shown in Figure 35(d). The level of the threshold magnitude needs to be carefully defined (to be detailed later in Section 4.3.2).

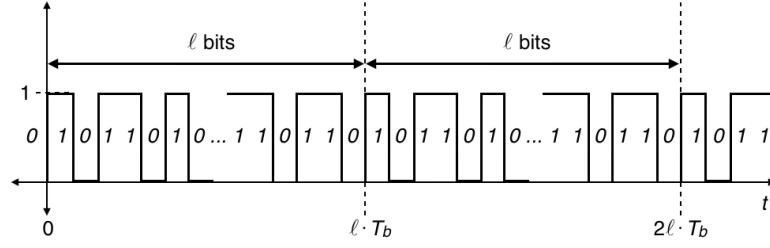
In addition, in the discrete power spectrum, some high frequency components may fall back near the fundamental frequency component due to sub-sampling and the resultant signal aliasing. For this reason, aliased frequency components also need to be carefully considered (to be described later in Section 4.3.3).

\*Assuming that the threshold magnitude and spectral components aliasing issues (shortly described above) can be resolved later in Section 4.3.2 and Section 4.3.3 respectively, the remaining part of the  $f_d$  coarse estimation algorithms is only described in this section. The spectral term denoted by  $f_d$  in Figure 35(d), in fact, consists of a few significant values (not a single value) due to the incoherent sampling and the noise of sampled signals. To accurately estimate the value of  $f_d$ , the interpolation technique three-point estimation is used [20].

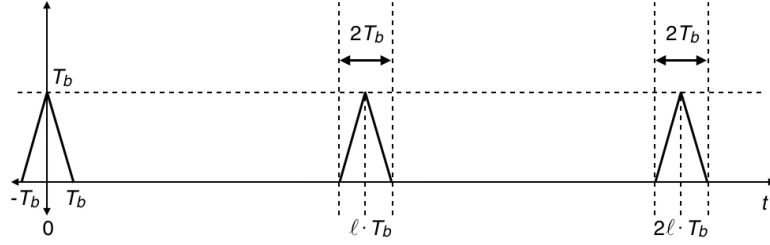
$$\dot{f}_d = \Delta_f \cdot \left( m + \frac{\ln \frac{X[m+1]}{X[m-1]}}{2 \cdot \ln \frac{X[m]^2}{X[m+1]X[m-1]}} \right), \quad (35)$$

where  $m$  is the discrete frequency index of the spectral peak, and  $\Delta_f$  is the DFT spectral resolution.

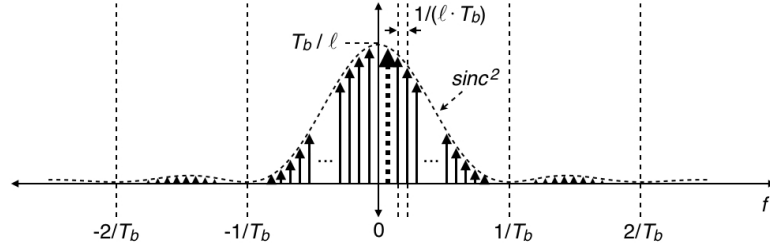
Even though the discrete frequency estimation described above is intended to be performed as accurately as possible, the estimation accuracy is degraded by the complex PRBS spectrum and its limited spectral resolution ( $\Delta_f$ ), hence it is called  $f_d$  coarse estimation.



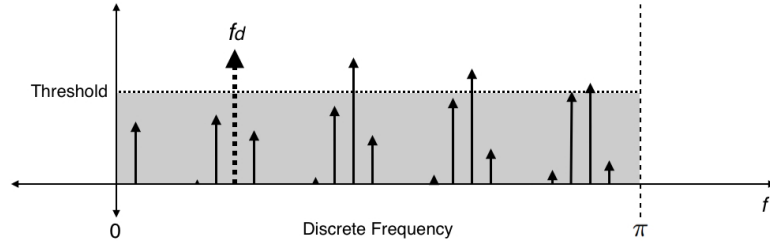
(a)  $l$ -bit PRBS shown in the time domain ( $T_b$  is the bit width).



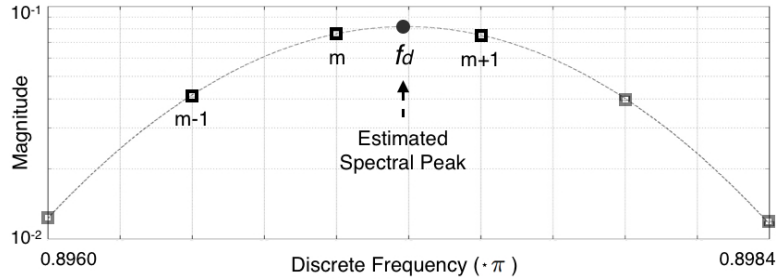
(b) Autocorrelation of the PRBS shown in Figure 35(a).



(c) Power spectrum of the continuous-time PRBS shown in Figure 35(a).



(d) Discrete power spectrum of the incoherently sub-sampled PRBS.



(e) Three-point estimation: the three spectral components (denoted by squares) near the discrete spectral peak of the fundamental tone (denoted by  $m$ ) of the discrete power spectrum of the incoherently sub-sampled PRBS.

**Figure 35:** Derivation of the power spectrum of a PRBS.

#### 4.1.2 Time Re-Mapping

The point samples of the discrete-time PRBS can be re-mapped (or reconstructed) into a single period waveform, which is represented in the discrete-time domain ranging from 0 to 2, by using the estimated discrete frequency value  $\dot{f}_d$  obtained from Section 4.1.1. The discrete-time value of the  $k$ -th sample point,  $t_d[k]$ , is defined as

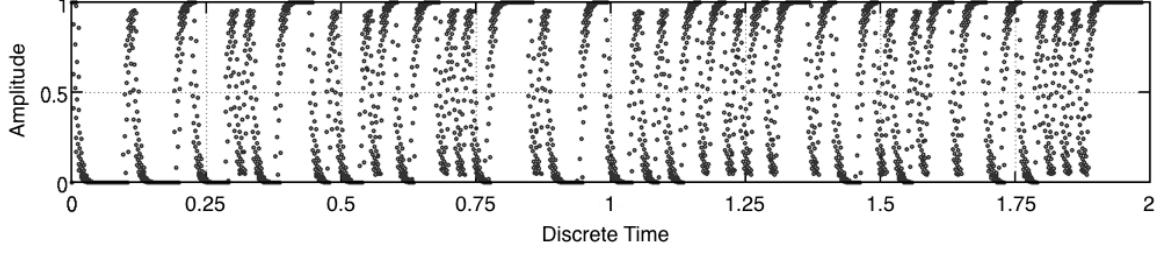
$$t_d[k] = \text{mod}(t_d[k-1] + \dot{f}_d/\pi, 2), \quad (36)$$

where the modulo operation  $\text{mod}(x, y)$  returns  $(x - n \cdot y)$ , and  $n$  is the greatest integer less than or equal to  $(x/y)$ . Equation 36 is identical to Equation 24 in Section 3.1.2.2.

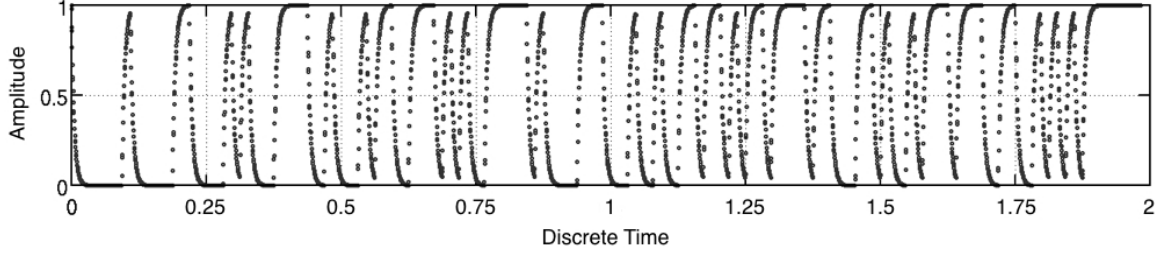
In computer simulation, a  $\approx 3.23$ -Gbps 127-bit PRBS was sub-sampled at 1-Gsps, and the obtained sample points were re-mapped to the discrete-time domain using Equation 35 and Equation 36. The re-mapped waveform is shown in Figure 36(a). As shown in the figure, the re-mapped waveform contains timing distortion shown as horizontal dispersion of the samples. Since the original continuous-time PRBS does not contain jitter (in the simulation), the timing distortion of the re-mapped waveform is solely induced by errors in the coarse discrete frequency estimation.

#### 4.1.3 Discrete Frequency Fine Estimation

The reconstructed PRBS using the coarse frequency estimate may involve reconstruction errors, which in turn result in the discrete-time dispersion of the point samples of the reconstructed PRBS as shown in Figure 36(a). In this section, the reconstruction errors are reduced by using a more accurate  $f_d$  estimate, hence the procedure is called  $f_d$  fine estimation. In the  $f_d$  fine estimation, the best estimate of  $f_d$  can be found when the spectral leakage of the discrete spectrum of the reconstructed PRBS is minimized. The reconstructed PRBS with discrete-time dispersion, shown in Figure 36(a), contains spectral leakage in its discrete spectrum as shown in Figure 37(a) (denoted by light grey circles).



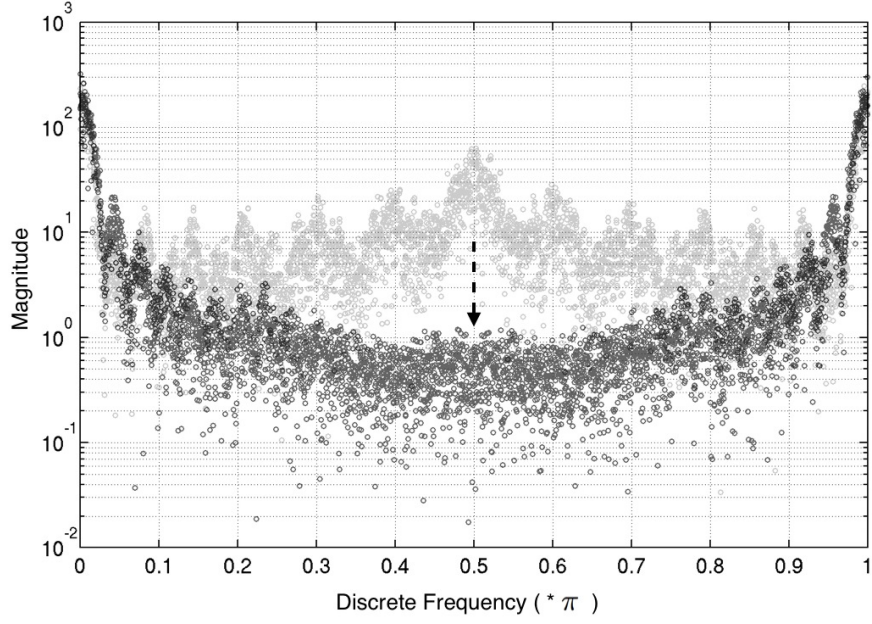
(a) Reconstructed waveform using the discrete frequency value determined by the *coarse* estimation.



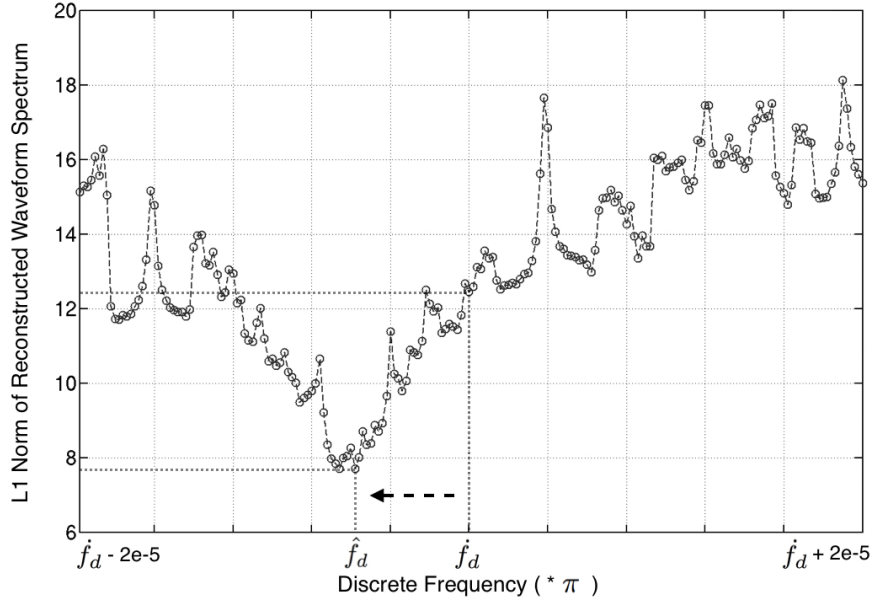
(b) Reconstructed waveform using the discrete frequency value determined by the *fine* estimation.

**Figure 36:** Simulation results for the proposed algorithms of discrete frequency measurement: A  $\approx 3.23$ -Gbps 127-bit digital signal without jitter is sampled at 1-Gsps.

The best reconstructed PRBS can be found by sweeping the discrete frequency value in the range of  $[\dot{f}_d - \Delta f_d/2, \dot{f}_d + \Delta f_d/2]$  where  $\Delta f_d$  is a discrete frequency deviation and  $\dot{f}_d$  denotes the coarsely estimated discrete frequency value. Among many different versions of the reconstructed PRBS obtained by sweeping the discrete frequency, the one with the least discrete spectral leakage (or the sparsest spectrum) is considered the best reconstructed PRBS [2]. Note that  $l_1$  norm is used to quantize the spectral sparsity. In Figure 37(b), the  $l_1$  norm values of the discrete spectra of reconstructed PRBSs are shown over various discrete frequency values ( $\Delta f_d/\pi = 4e-5$ ). By searching for the least  $l_1$  norm, the coarsely estimated value  $\dot{f}_d$  is corrected to the fine estimation value  $\hat{f}_d$ . The reconstructed PRBS using the fine estimation of  $\hat{f}_d$  is shown in Figure 36(b), and its spectrum is shown in Figure 37(a) (denoted by dark grey circles). In Figure 37(a), the discrete spectrum of the best reconstructed PRBS is more sparse in comparison with that of the reconstructed PRBS with reconstruction errors.



(a) Signal sparsity promotion: the spectrum of Figure 36(a) denoted by the marks with light grey and the spectrum of Figure 36(b) indicated by the marks with dark grey.



(b) The  $l_1$  norm values of the spectrum of reconstructed waveforms are shown over various discrete frequency values utilized for the signal reconstruction.

**Figure 37:** Simulation results for the proposed algorithms of discrete frequency measurement: A  $\approx 3.23$ -Gbps 127-bit digital signal without jitter is sampled at 1-Gsps.

#### 4.1.4 Long-Term Jitter Compensation

Random jitter accumulates over time and behaves as a random walk, which is unbounded and contains long-term (trend) components as well as short-term components. When a PRBS with random jitter is tested for jitter, the jitter measurements need to be carefully compensated for the long-term jitter of the PRBS. Conventional oscilloscopes use a phase-synchronized sampling time-base which is recovered from the input signal being sampled. Because of the synchronization, the time-base signal contains the same long-term jitter content as that of the test signal. For this reason, the long-term jitter of the test signal is automatically cancelled out and not measured by the oscilloscope. By contrast, the proposed jitter characterization technique does not incorporate phase-synchronization hardware so that long-term jitter content needs to be separately compensated in digital post-processing. Otherwise, the reconstructed waveform from the signal reconstruction process (described in Section 4.1) may be dispersed (in the discrete-time domain) to the extent that the waveform is hardly recognizable (especially in cases where long-term jitter contents are predominant). To address this issue, we propose to digitally compensate the reconstructed waveform for its long-term jitter components. Details of the long-term jitter compensation are described in the following.

Long-term jitter can be estimated by measuring the *time-varying* discrete frequency of a sampled signal, as compared to the *time-invariant* discrete frequency estimation  $\dot{f}_d$  used in Section 4.1. To perform such time-frequency analysis, we use the short-time Fourier transform (STFT) algorithm. In this method, the Fourier transform of local selections of the sampled signal is performed using a sliding time window. The discrete frequency of each local selection is estimated using the algorithms used in Section 4.1. However, the estimated value of discrete frequency may vary over the time windows due to the long-term jitter of the sampled signal (The relation between the jitter components of a signal and the frequency components of

the signal is described later in this section). The obtained discrete frequency estimations over the time windows form a *time-varying* discrete frequency value, which is used for the long-term jitter compensation.

In computer simulation, a  $\approx 27.69$  psec rms random jitter time series was generated as shown in plot (a) of Figure 39(a), and this jitter time series was injected to the time-base of a  $\approx 3.23$ -Gbps, 127-bit PRBS. The PRBS was then incoherently subsampled at 1-Gsps (without sampling jitter), and  $2^{14}$  samples were acquired. From the sampled data, the time-varying discrete frequency value  $\hat{f}_d[k]$  ( $k$  is the sample index) was estimated using the STFT. The obtained  $\hat{f}_d[k]$  was then transferred to the discrete time value  $t_d[k]$  using Equation 37.

$$t_d[k] = \text{mod}(t_d[k-1] + \hat{f}_d[k]/\pi, 2). \quad (37)$$

Note that Equation 37 is a modified version of Equation 36. Plot (b) of Figure 39(a) shows the long-term jitter estimation, which is obtained by rescaling the variation in  $t_d[k]$  to the continuous time domain for comparison purposes. It is clear from the figure that plot (b) tracks the long-term movement of plot (a). Figure 38(a) shows the reconstructed PRBS with long-term jitter compensation, showing less discrete-time dispersion. In addition, the known long-term jitter characteristics can be provided separately as supporting jitter information.

## 4.2 Jitter Quantization in the Reconstructed Discrete-Time Domain

### 4.2.1 Self-Reference Signal Extraction

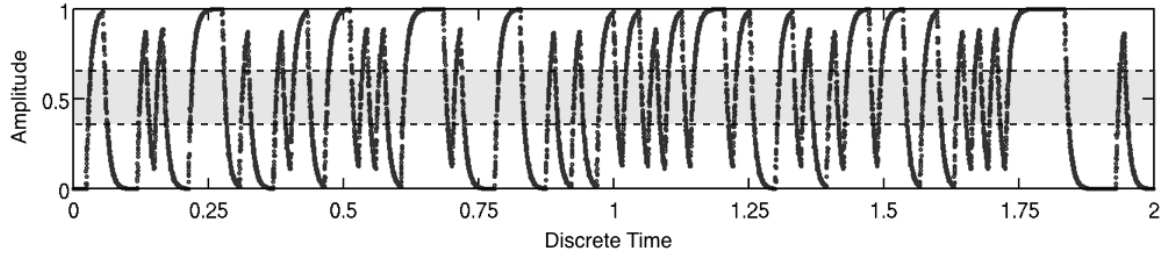
To enable accurate jitter measurement (or quantization), a timing reference signal is mandatory. In this research, however, a timing reference signal is not explicitly provided. Rather, a self-reference signal is extracted from the sampled PRBS itself by using signal denoising techniques. The use of the (digitally obtained) self-reference signal alleviates the need for additional signal sources and timing circuitry.

We use wavelet shrinkage to denoise a reconstructed waveform and find its self-reference waveform. A discrete wavelet transform (DWT) is widely used to denoise a randomly distorted signal in the discrete wavelet domain. Especially for phase noise reduction (as compared to amplitude noise reduction), the noise suppression performance of wavelet shrinkage methods has been evaluated in many relevant areas [9, 25, 37, 65] (Note that jitter is considered phase noise in digital signals). These techniques use the fact that wavelet coefficients at low-frequency scales are dominated by signal concentration, whereas those at high-frequency scales mainly represent signal noise components. In this research, we apply the wavelet shrinkage to the reconstructed PRBS to compensate the signal for high-frequency noise including short-term jitter-induced noise so that we consecutively obtain the self-reference signal.

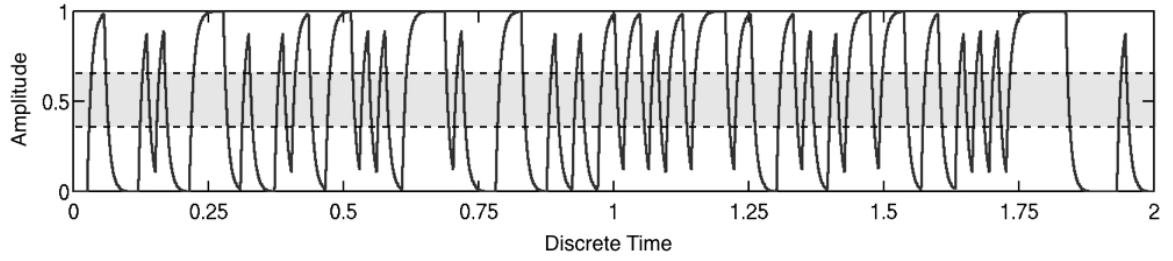
In the computer simulation previously described in Section 4.1.4, Figure 38(a) shows the reconstructed waveform whose point samples contain discrete-time errors (or dispersion) due to jitter of the original PRBS being sampled. Figure 38(b) shows the self-reference signal obtained by denoising the reconstructed PRBS using the wavelet shrinkage with the Daubechies 4-tap wavelet and 6-level decomposition. Figure 38(c) shows an enlarged view of both the reconstructed signal and the self-reference signal.

To evaluate the performance of the self-reference signal extraction, we compared various self-reference signals (obtained by using various wavelets) with an ideal reference signal, which is only available in computer simulation. Timing differences between the self-reference signals and the ideal reference signal were measured in unit intervals (UIs). Table 4 shows timing comparison results for various wavelets and decomposition levels (30% of the signal dynamic range was considered for the timing comparison as indicated in Figure 38).

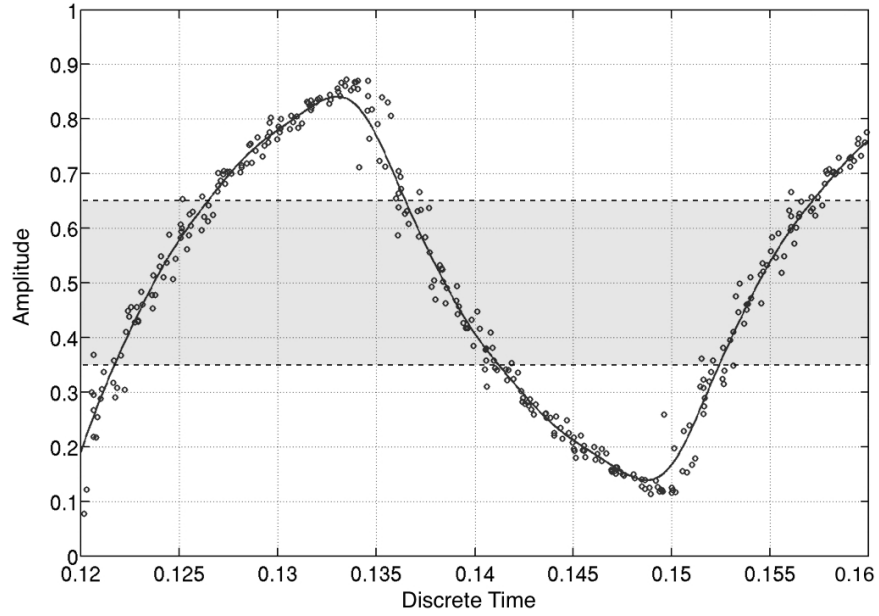




(a) Reconstructed waveform (denoted by circular marks) of a 127-bit digital pattern with jitter.

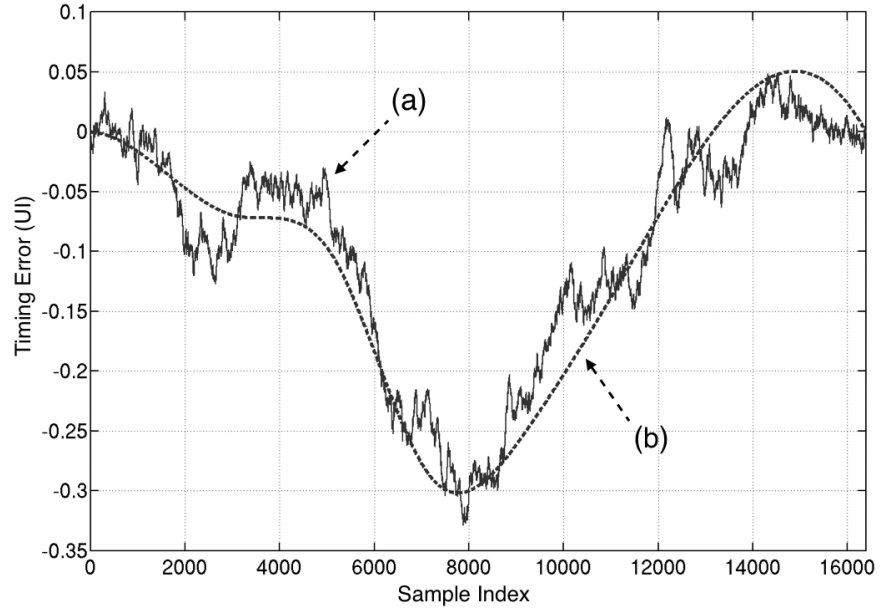


(b) Self-reference signal (denoted by a solid line) extracted from the reconstructed signal in Figure 38(a).

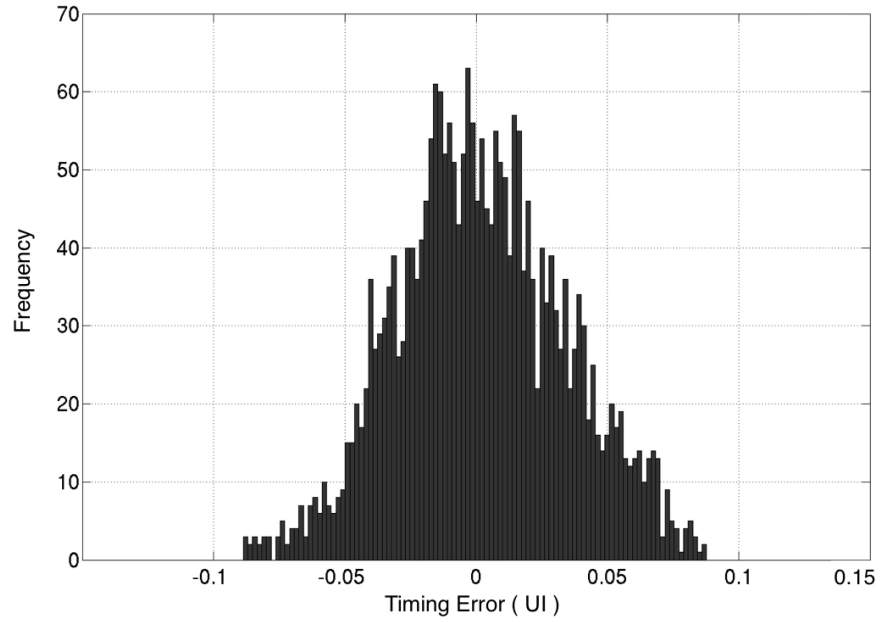


(c) Enlarged view of the signals both of Figure 38(a) and Figure 38(b).

**Figure 38:** Simulation results of a  $\approx 3.23$ -Gbps 127-bit digital signal with injected jitter, sampled at 1-Gsps.



(a) Original jitter values injected to the PRBS, denoted by (a), and software CR based jitter tracking results, denoted by (b), are partially shown.



(b) Jitter Histogram of the reconstructed signal of Figure 38(a).

**Figure 39:** Simulation results of a  $\approx 3.23$ -Gbps 127-bit digital signal with injected jitter, sampled at 1-Gsps (continued from Figure 38).

**Table 4:** Self-reference signals' absolute timing errors measured in UIs.

Wavelet (Decomposition Level)	Mean ( $\cdot 10^{-3}$ )	Max ( $\cdot 10^{-3}$ )	RMS ( $\cdot 10^{-3}$ )
Harr (4)	0.0469	0.1193	0.0319
Harr (5)	0.0430	0.1193	0.0285
Daubechies 2 (4)	0.0483	0.1232	0.0336
Daubechies 2 (5)	0.0410	0.0993	0.0256
Daubechies 4 (4)	0.0495	0.1276	0.0348
Daubechies 4 (5)	0.0409	0.0927	0.0251
Biorthogonal 1.3 (4)	0.0483	0.1232	0.0336
Biorthogonal 1.3 (5)	0.0410	0.0993	0.0256
Discrete Meyer (4)	0.0508	0.1307	0.0360
Discrete Meyer (5)	0.0416	0.0844	0.0242

#### 4.2.2 Jitter Quantization

Sections 4.1 and 4.2.1 showed that the reconstructed PRBS contains discrete-time dispersion due to jitter of the original continuous-time PRBS being sampled and that the self-reference signal can be digitally generated. In this section, we measure the jitter of the continuous-time PRBS by quantifying the discrete-time dispersion and dislocation of the point samples of the reconstructed PRBS.

For random jitter measurement, the discrete-time dispersion of the reconstructed PRBS from the self-reference signal (given by Section 4.2.1) is quantified. In this scheme, the data-dependent jitter of the PRBS is automatically excluded from the categories of jitter being measured since the data-dependent jitter content is present both in the reconstructed PRBS and the self-reference signal. Figure 38(c) provides an enlarged view of the reconstructed PRBS and its self-reference signal (provided by the computer simulation in Section 4.2.1) and indicates that the point samples within a pre-defined amplitude range (30% of the dynamic range) are examined when the discrete-time dispersion of the samples is quantified. This is because the point samples adjacent to the amplitude levels of logic high and low are more affected by amplitude noise rather than timing noise [31, 55]. The quantization process is repeated for all the transition edges of the reconstructed PRBS, and the obtained

values are shown in Figure 39(b) using jitter histogram, which directly corresponds to the vertical distances between plot (a) and plot (b) of Figure 39(a). The jitter histogram of Figure 39(b) indicates that the reconstructed PRBS contains  $\approx 0.0309$  UI rms random jitter in the discrete-time domain, and the fact consequently implies that the original continuous-time PRBS being sampled contains  $\approx 9.55$  psec rms random jitter *subsequent to* the long-term jitter compensation. In cases where the long-term jitter contents also need to be measured, the values of plot (b) of Figure 39(a), which are the long-term jitter contents, can be simply added to the jitter values obtained from the reconstructed PRBS, resulting in a jitter value of  $\approx 27.23$  psec rms (The PRBS being sampled originally contained  $\approx 27.69$  psec rms random jitter).

As compared to the random jitter measurement, the data-dependent jitter of the reconstructed PRBS is measured by observing the zero-crossing time variations of the self-reference signal, not the reconstructed PRBS. This is because the self-reference signal contains the same data-dependent jitter as that of the reconstructed PRBS since the self-reference signal is a moving average (in time and amplitude) of the samples of the reconstructed PRBS. To evaluate the performance of the data-dependent jitter measurement using the self-reference signal, we compared among data-dependent jitter values of self-reference signals obtained by using various wavelets: Harr, Daubechies, Biorthogonal, and Discrete Meyer. The comparison results are summarized in Tables 5 and 6.

One of the benefits of using the proposed jitter quantization is that jitter values of each transition edge of a reconstructed PRBS are measured separately so that data-dependent jitter can be automatically decomposed from total jitter. In comparison, conventional jitter analyzers collect jitter information from all the transition edges of the PRBS being sampled (without edge distinction) and then decompose the obtained total jitter information into jitter sub-subcategories using histogram-based jitter decomposition methods [11, 34].

**Table 5:** Data-dependent jitter estimations, measured in UIs, obtained by using various self-reference signals (rising edges only).

Signal Edges	Harr (6)	Db2 (6)	Db4 (6)	Bior1.3 (6)	DMey (6)
e01	0.0147	0.0150	0.0158	0.0150	0.0165
e03	0.0119	0.0118	0.0122	0.0118	0.0125
e05	-0.0386	-0.0382	-0.0380	-0.0382	-0.0380
e07	0.0181	0.0181	0.0184	0.0181	0.0186
e09	0.0127	0.0114	0.0111	0.0114	0.0109
e11	0.0180	0.0176	0.0180	0.0176	0.0189
e13	-0.0322	-0.0318	-0.0312	-0.0318	-0.0299
e15	0.0134	0.0120	0.0114	0.0120	0.0106
e17	-0.0454	-0.0453	-0.0455	-0.0453	-0.0456
e19	-0.0295	-0.0296	-0.0296	-0.0296	-0.0285
e21	0.0237	0.0237	0.0238	0.0237	0.0233
e23	-0.0351	-0.0350	-0.0348	-0.0350	-0.0338
e25	0.0254	0.0255	0.0260	0.0255	0.0260
e27	0.0322	0.0323	0.0327	0.0323	0.0330
e29	0.0237	0.0235	0.0238	0.0235	0.0243
e31	0.0275	0.0259	0.0254	0.0259	0.0251
e33	-0.0269	-0.0277	-0.0284	-0.0277	-0.0292
e35	-0.0268	-0.0263	-0.0260	-0.0263	-0.0248
e37	-0.0248	-0.0246	-0.0244	-0.0246	-0.0236
e39	-0.0337	-0.0355	-0.0365	-0.0355	-0.0372
e41	-0.0233	-0.0231	-0.0230	-0.0231	-0.0222
e43	0.0345	0.0340	0.0340	0.0340	0.0333
e45	-0.0278	-0.0276	-0.0276	-0.0276	-0.0271
e47	0.0338	0.0335	0.0337	0.0335	0.0339
e49	-0.0101	-0.0104	-0.0108	-0.0104	-0.0110
e51	-0.0234	-0.0236	-0.0240	-0.0236	-0.0248
e53	0.0386	0.0389	0.0393	0.0389	0.0397
e55	0.0399	0.0380	0.0375	0.0380	0.0374
e57	-0.0078	-0.0090	-0.0095	-0.0090	-0.0098
e59	-0.0109	-0.0112	-0.0116	-0.0112	-0.0116
e61	-0.0048	-0.0043	-0.0039	-0.0043	-0.0031
e63	0.0277	0.0275	0.0274	0.0275	0.0267

**Table 6:** Data-dependent jitter estimations, measured in UIs, obtained by using various self-reference signals (falling edges only).

Signal Edges	Harr (6)	Db2 (6)	Db4 (6)	Bior1.3 (6)	DMey (6)
e02	0.0095	0.0100	0.0102	0.0100	0.0098
e04	-0.0498	-0.0490	-0.0494	-0.0490	-0.0500
e06	-0.0431	-0.0427	-0.0430	-0.0427	-0.0438
e08	0.0118	0.0107	0.0105	0.0107	0.0101
e10	-0.0478	-0.0480	-0.0484	-0.0480	-0.0492
e12	-0.0448	-0.0436	-0.0434	-0.0436	-0.0431
e14	0.0101	0.0093	0.0089	0.0093	0.0082
e16	0.0281	0.0288	0.0294	0.0288	0.0296
e18	-0.0330	-0.0322	-0.0320	-0.0322	-0.0314
e20	-0.0335	-0.0335	-0.0337	-0.0335	-0.0334
e22	0.0285	0.0291	0.0297	0.0291	0.0303
e24	-0.0226	-0.0224	-0.0223	-0.0224	-0.0220
e26	0.0285	0.0284	0.0287	0.0284	0.0288
e28	-0.0330	-0.0320	-0.0322	-0.0320	-0.0327
e30	-0.0356	-0.0348	-0.0350	-0.0348	-0.0353
e32	0.0254	0.0256	0.0256	0.0256	0.0248
e34	0.0293	0.0300	0.0306	0.0300	0.0314
e36	-0.0203	-0.0195	-0.0193	-0.0195	-0.0184
e38	0.0292	0.0282	0.0275	0.0282	0.0262
e40	0.0397	0.0397	0.0400	0.0397	0.0405
e42	0.0350	0.0352	0.0351	0.0352	0.0342
e44	0.0368	0.0370	0.0375	0.0370	0.0380
e46	-0.0126	-0.0120	-0.0118	-0.0120	-0.0113
e48	-0.0209	-0.0206	-0.0211	-0.0206	-0.0215
e50	0.0471	0.0465	0.0462	0.0465	0.0458
e52	0.0474	0.0483	0.0488	0.0483	0.0488
e54	0.0326	0.0327	0.0330	0.0327	0.0329
e56	-0.0200	-0.0195	-0.0197	-0.0195	-0.0203
e58	-0.0064	-0.0067	-0.0075	-0.0067	-0.0085
e60	-0.0086	-0.0074	-0.0073	-0.0074	-0.0070
e62	0.0414	0.0421	0.0427	0.0421	0.0425
e64	-0.0433	-0.0434	-0.0439	-0.0434	-0.0444

## 4.3 More Considerations

### 4.3.1 PSDs of Time-Base Signals With Jitter

The power spectral density (PSD) of a (sinusoidal) time-base signal of a PRBS with jitter is discussed *before* and *after* the long-term jitter compensation is applied to the signal reconstruction. Plots (a) and (b) of Figure 40(a) respectively show a jitter time series (to be injected to the time-base of a PRBS) and the long-term jitter detection of that jitter time series (obtained by using the long-term jitter compensation in Section 4.1.4). Note that, in Figure 40(a), plot (b) does not follow plot (a) at any frequency from 1 to 10 MHz. This indicates that only the long-term (low-frequency) jitter can be detected and compensated for using the long-term jitter compensation algorithms. Plots (a) and (b) of Figure 40(b) respectively show the PSDs of plots (a) and (b) of Figure 40(a). As shown in plot (a) of Figure 40(b), the PSD of a random jitter time series shows a wideband spectrum due to random nature of jitter. The wideband jitter can be separated into short-term jitter and long-term jitter components with regards to its variation frequency. The long-term jitter corresponds to spectral components of jitter in low-frequency bands as compared to the short-term jitter relating to the spectral components in high-frequency bands.

Appendix E shows that the PSD of a jitter time series can be converted to the PSD of a sinusoidal signal with that jitter time series by deterministically modeling jitter (or phase noise) using a linear chirp modulation tone with time-varying amplitude. In Appendix E, the PSD (one-sided) of a (deterministically modeled) phase noise function  $\Delta\phi_n(t)$  is given by

$$S_{\Delta\phi_n}(\omega) = \sum_{i=0}^{n-1} \frac{A_i^2}{2n} \cdot \delta(\omega - \beta \cdot i), \quad (38)$$

where  $A_i$  are the time-varying amplitudes of the  $\Delta\phi_n(t)$ ,  $\beta$  is the resolution bandwidth (RBW),  $\beta \cdot n$  is the phase noise bandwidth of interest. The PSD (one-sided) of a carrier

signal phase-modulated by the function  $\Delta\phi_n(t)$  is given by

$$\begin{aligned}
S_{y_{cn}} = & \underbrace{\left[ \frac{A_c^2}{2n} + \sum_{i=1}^{n-1} \frac{(J_0(A_i) \cdot A_c)^2}{2n} \right]}_{\text{carrier}} \cdot \delta(\omega - \omega_c) \\
& + \underbrace{\sum_{j=1}^{\infty} \sum_{i=1}^{n-1} \frac{(J_j(A_i) \cdot A_c)^2}{2n} [\delta(\omega - (\omega_c + \beta \cdot i)) + \delta(\omega - (\omega_c - \beta \cdot i))]}_{\text{side-bands}}. \quad (39)
\end{aligned}$$

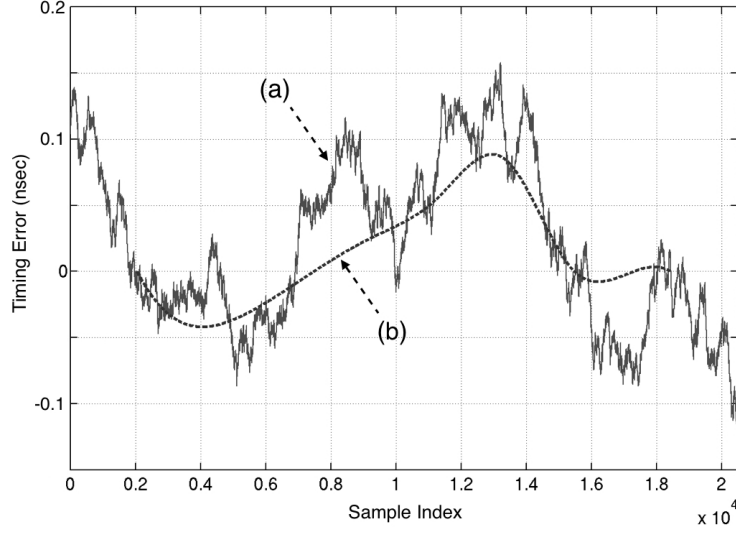
where  $\omega_c$  is the carrier signal angular frequency, and the function  $J_\alpha(x)$  is the Bessel function of the first kind (See Appendix E for details of the models). Using this relation, we performed a computer simulation to show that how much jitter can be compensated for in terms of the PSD of a (sinusoidal) time-base signal of a PRBS. Plot (a) and (b) of Figure 40(c) respectively show the PSDs of (sinusoidal) time-base signals (whose carrier power levels are 1) with the jitter time series (a) and (b) in Figure 40(b). The long-term jitter content of the time-base signal (mostly) contributes to the power spectrum of the signal at small offset frequencies, resulting in close-in phase noise, while the short-term jitter content contributes to the power spectrum at large offset frequencies, providing far-out phase noise.

#### 4.3.2 Sub-Sampling Ratio Selection

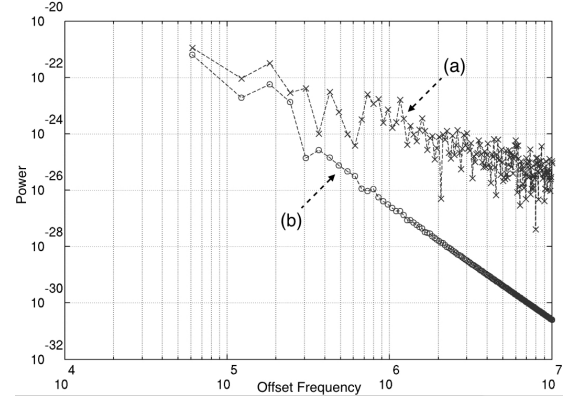
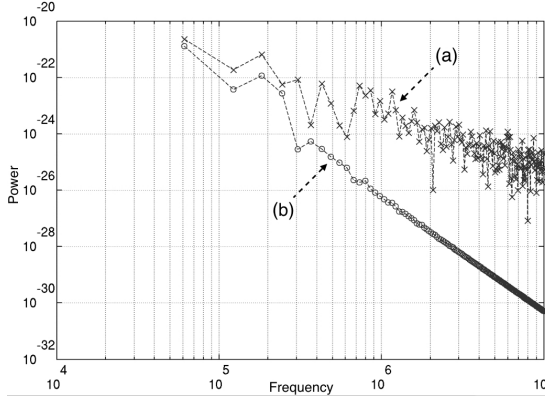
The sub-sampling ratio of the proposed signal acquisition needs to be carefully determined (the definition of sub-sampling ratio is given by Appendix D). In case the sub-sampling ratio is too small, the discrete spectrum of the sampled signal is too complex to analyze for the discrete frequency estimation. This increased complexity also makes test automation difficult. To address such challenges, details of the sampling ratio determination process are described in the following.

There exist a few issues to be considered with regard to determining a sub-sampling ratio. First, the PRBS to be sub-sampled is not an ideal waveform. The PSD of an ideal PRBS (with an infinite slew rate and infinitely long bit pattern) shows a series of the Dirac delta functions with the envelope given by the square of the sinc





(a) Plots (a) and (b) respectively show a jitter times series (injected to a PRBS time-base) and software CR based jitter tracking.



(b) Plots (a) and (b) respectively show the PSD (one-sided) estimations of the jitter time series (one-sided) estimations of carrier signals with the (a) and (b) of Figure 40(a).

**Figure 40:** Simulation results of the software CR based jitter tracking.

function (as shown in Figure 35(c)). In practice, the discrete PSD of a sampled PRBS, however, is not identical to that in Figure 35(c). The PSD of the practical PRBS may be deviated from the ideal due to the limited slew rate, finite pattern length and the finite number of sample points. Second, the frequency components of the PSD are aliased with multiple folds in the discrete-frequency domain. These aliased frequency components may complicate the overall PSD plot when they are located (in the discrete-frequency domain) close to the fundamental frequency components of comparable power levels. These issues can be addressed by giving a margin to the sub-sampling ratio when (incoherently) sub-sampling a non-ideal PRBS.

### 4.3.3 Line Spectra Overlapping

The discrete PSD of a sub-sampled PRBS shows multiple frequency components (or line spectra) which are aliased in the discrete frequency domain due to sub-sampling. In some cases, the line spectra are overlapped on the top of each other so that the PSD of such a sampled signal is less informative in terms of the discrete frequency estimation. Consequently, the accuracy of the discrete frequency estimation is compromised.

The PSD of a continuous-time PRBS is shown in Figure 41(a) and compared with its discrete PSD (shown in Figure 41(b)) obtained from (incoherently) sub-sampling the PRBS. In Figure 41(a), the frequency locations (a) and (b) are apart from  $f_s$  by  $f_b/l$ , and the (c) and (d) are apart from  $2f_s$  by  $f_b/l$ . In Figure 41(b), these frequency locations are relocated (or converged) to the discrete fundamental frequency  $f_d (= (f_b/l)/(f_s/2) \cdot \pi)$  due to signal aliasing. Similarly, the frequency components (of a continuous-time PRBS) near the frequency location of  $\lambda \cdot f_s \pm f_b/l$  ( $\lambda = 1, 2, \dots$ ) are aliased near to the discrete fundamental frequency  $f_d$  (in the discrete frequency domain) when the signal is sub-sampled. If the aliased terms are located too close to the  $f_d$ , identifying the location of the  $f_d$  is problematic and hence line spectra

overlapping. For instance, the frequency components (1) to (8) in Figure 41(a) are sub-sampled and aliased near to the  $f_d$  in the discrete frequency domain as shown in Figure 41(b). In particular, the discrete frequency component (4) is located very close to the  $f_d$ , distorting the discrete spectrum information of the fundamental frequency  $f_d$ .

To prevent the discrete line spectra from being overlapped on the fundamental frequency component, the sampling criterium is given as below.

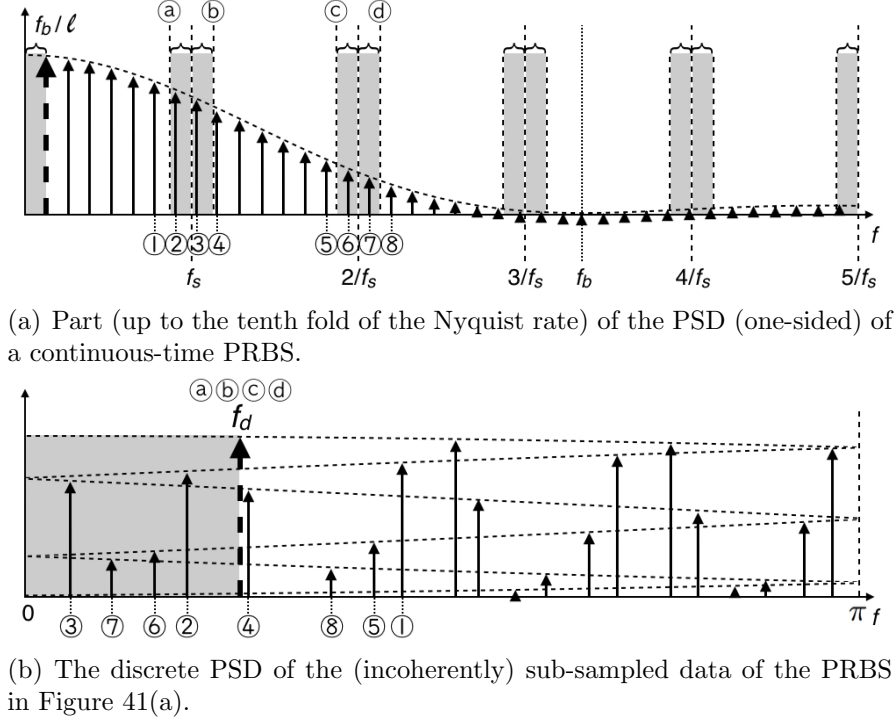
$$\min \left( \begin{aligned} &|\lambda \cdot f_s - f_b/l - \beta \cdot f_b/l|, \\ &|\lambda \cdot f_s - f_b/l - (\beta + 1) \cdot f_b/l|, \\ &|\lambda \cdot f_s + f_b/l - (\beta + 2) \cdot f_b/l|, \\ &|\lambda \cdot f_s + f_b/l - (\beta + 3) \cdot f_b/l| \end{aligned} \right) > 2f_s/n, \quad (40)$$

where

$$\beta = \lfloor \frac{\lambda \cdot f_s - f_b/l}{f_b/l} \rfloor, \quad (41)$$

$$\lambda = 1, 2, \dots, \lfloor f_b/f_s + 1 \rfloor, \quad (42)$$

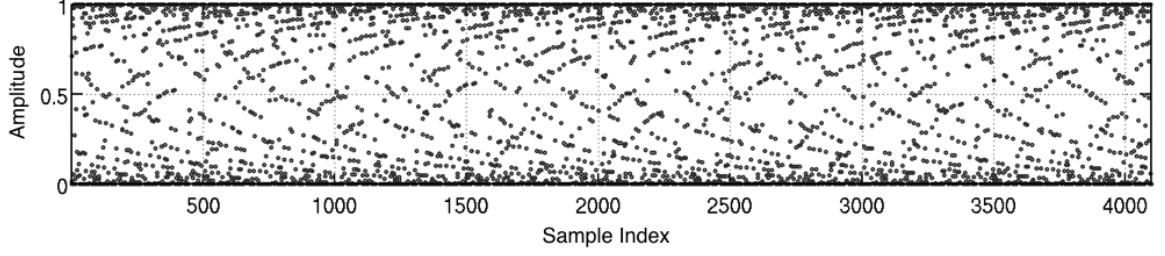
$f_b$  and  $l$  are the bit frequency and pattern length of the PRBS respectively,  $f_s$  is the sampling speed, and  $\lfloor \cdot \rfloor$  is the floor function which maps a real number to the next smallest integer. Equation 40 indicates that the distance in frequency between  $\lambda \cdot f_s \pm f_b/l$  ( $\lambda = 1, 2, \dots$ ) and nearby frequency components needs to be always larger than  $2f_s/n$ , twice the frequency resolution of the discrete PSD. Note that the frequency components located at the distance of  $f_s/n$  (from the fundamental tone) is considered to result in the line spectra overlapping since it negatively contributes to the fundamental frequency estimation process (refer to the three-point calculation in the fundamental frequency estimation described in Section 4.1.1). In addition, the spectrum up to  $f_b$  is only considered as indicated in Equation 42 assuming that the power level of the spectrum beyond  $f_b$  is low enough to be negligible.



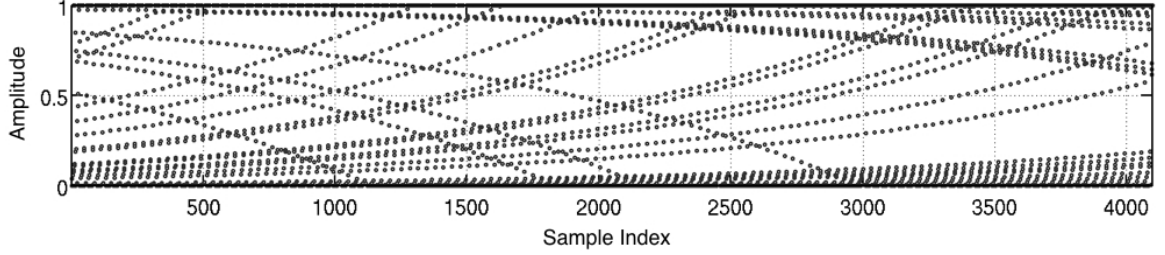
**Figure 41:** Line spectra overlapping with the fundamental discrete frequency component.

Using computer simulation, an example of the information-rich sampled PRBS is shown in Figure 42(a). The PSD of this signal does not have frequency components that are overlapped (except the terms whose power level is close to the noise floor) as shown in Figure 43(a) so that the fundamental frequency component is clearly identified. In comparison, Figure 42(b) shows a sampled PRBS whose sample points are sparsely distributed (in terms of amplitude) within a local selection of sample index. The PSD of this sampled signal, as shown in Figure 43(b), contains overlapped (or sparse) frequency components so that it is less informative in terms of the discrete frequency estimation.

To prevent the line spectra overlapping, a sub-sampling digitizer with programmable sampling clocks can be used. By adjusting the sampling speed with a small amount, a possible line spectra overlapping issue is simply resolved.



(a) Raw sub-sampled waveform of a 3-Gbps 127-bit sequence, digitized at 727.17-Msps.

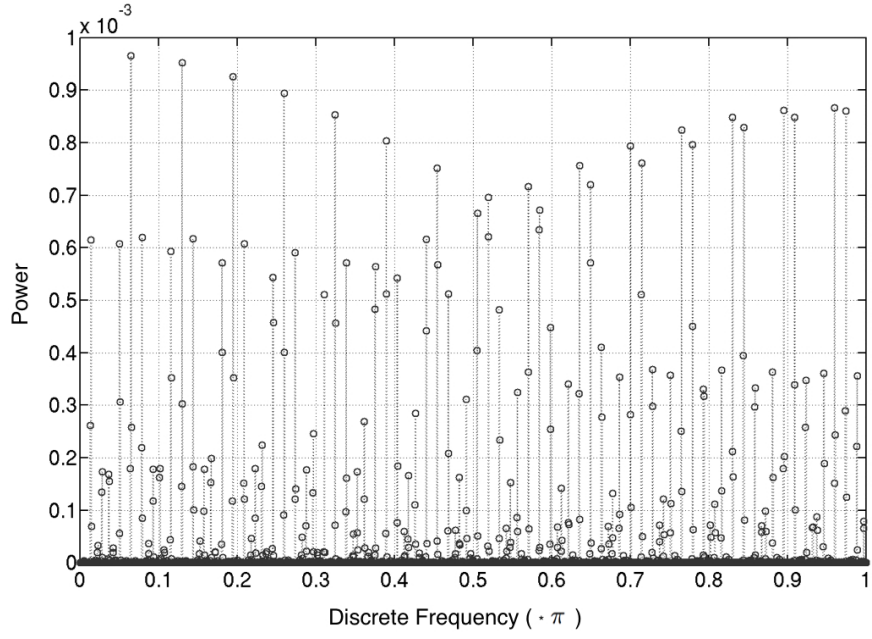


(b) Raw sub-sampled waveform of a 3-Gbps 127-bit sequence, digitized at 755.94-Msps (problematic sample distribution).

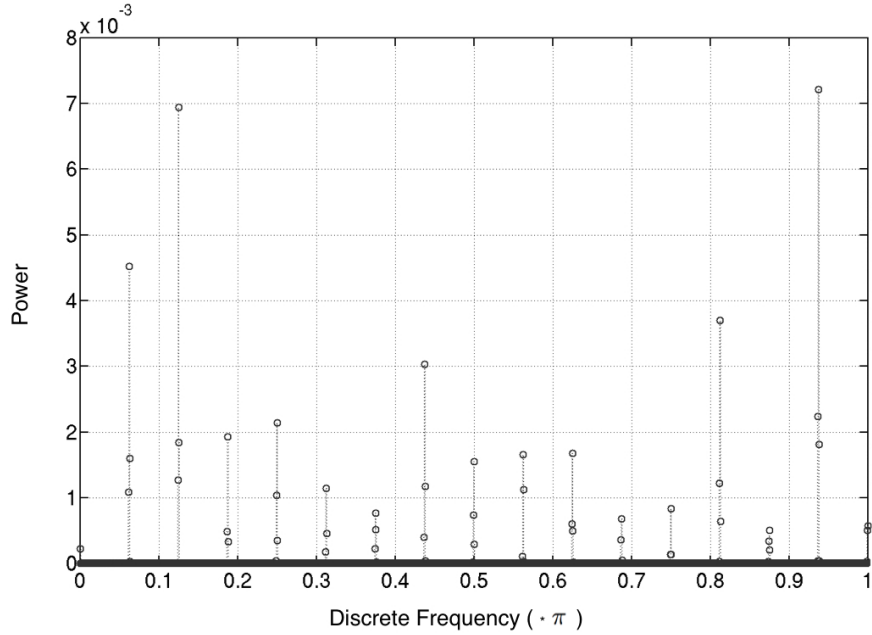
**Figure 42:** Simulation results (time-domain signal) for two cases of sub-sampling regarding sample distribution.

#### 4.4 Summary

This chapter presented a new methodology for jitter characterization of high-speed digital signals. To acquire digital signals being tested, we used incoherent sub-sampling to increase the effective sampling rate of a digitizer and to simplify the data acquisition hardware of the digitizer. The performance of the signal reconstruction and jitter characterization algorithms was evaluated with computer simulation.



(a) Discrete power spectrum (FFT-based, one-sided) of the sub-sampled waveform shown in Figure 42(a)



(b) Discrete power spectrum (FFT-based, one-sided) of the sub-sampled waveform shown in Figure 42(b) (problematic spectrum)

**Figure 43:** Simulation results (spectrum) for the two cases of sub-sampling shown in Figure 42(a) and Figure 42(b).

## CHAPTER V

### CONCLUSION

Throughout the previous three chapters, this dissertation focused on developing a jitter measurement methodology for high-speed digital signals. In conclusion, Section 5.1 clarifies the major contributions of this dissertation, emphasizing the applicability of the proposed method to jitter measurement and testing of high-speed digital signals. For further improvement of the proposed method, Section 5.2 presents the current limitations of the developed method and suggests future work to address the limitations. Section 5.3 shows technical papers and inventions published through the dissertation research.

#### 5.1 Contributions

This dissertation research focused on jitter characterization of high-speed digital (or analog) signals using narrow-bandwidth testers or simplified data acquisition hardware. Chapter 2 showed that the jitter sensor can expand jitter of digital signals being tested and that the expanded jitter can be measured with narrow-bandwidth testers. Chapters 3 and 4 showed that a simplified (without synchronization circuitry) signal acquisition module can incoherently sub-sample a high-speed signal and reconstruct the signal into a single-period waveform by using the back-end signal processing algorithms. The jitter of the reconstructed signal is then quantified in the digital domain. This signal acquisition and jitter characterization method uses a much simplified data acquisition topology compared to the conventional jitter analyzers, reducing the cost of jitter testing.

## 5.2 Future Work

The current contributions of this dissertation can be improved in their applicability to jitter measurement by completing the following future work.

- **Jitter decomposition using jitter expansion:** Jitter of a high-speed signal is reconstructed on a down-converted low-speed signal using a jitter sensor (i.e. envelope detector, mixer, sample-and-hold amplifier, etc.) The reconstructed jitter obtained by using the jitter sensor consists of random jitter as well as deterministic jitter as the jitter of the original high-speed signal does. To accurately characterize the reconstructed jitter and subsequently estimate the original jitter value, the reconstructed jitter needs to be digitally decomposed into its sub-categories. However, the waveform of the sensor output signal (containing the reconstructed jitter) depends not only on its deterministic jitter but on the jitter sensor topology being used. For this reason, a new jitter decomposition technique needs to be developed especially for the reconstructed jitter characterization. First, the reconstructed jitter is decomposed into two major jitter components: deterministic jitter and random jitter. Random jitter components of the original high-speed signal cause random timing variations on the down-converted low-speed signal, while deterministic jitter components result in systematic distortions. By distinguishing these two categories of jitter behavior in the reconstructed time domain, the reconstructed jitter can be decomposed. In addition, deterministic jitter can be further classified into data dependent jitter (or intersymbol interference), periodic jitter, and bounded uncorrelated jitter.
- **Optimization of signal reconstruction time:** The  $f_d$  fine measurement described in Section 4.1.3 can be optimized to reduce required computation time. Evaluating the spectrum of reconstructed signals for sparsity analysis as shown



in Figure 37(a) and 37(b) takes a considerable amount of computation time: the set of inherently nonequispaced samples in reconstructed signals requires nonequispaced DFT (NDFT) (time-consuming compared to regular DFT), and such NDFT needs to be performed on each reconstructed signal while sweeping  $\dot{f}_d$  [16, 28]. To resolve the computation time issue, a local minima search algorithm (instead of sweeping  $\dot{f}_d$ ) needs to be developed, and the regular DFT methods should be considered to replace the NDFT in case the sample size of signals is large.

- **Time-base modulated sub-sampling for acquisition of high-speed signals:** For data-efficient high-speed signal acquisition, an ultra high-speed sampling track-and-hold amplifier (THA) whose time-base signal is randomly modulated is used as the front-end of a sampling-based signal acquisition system. In this signal acquisition scheme, a high-speed signal being tested is randomly sampled by the THA at the Nyquist rate, and the output signal of the THA is then low-pass filtered and regularly re-sampled (or digitized) by a following low-speed ADC (relies on the theory of compressive sampling [38, 39, 47, 64]). The signal acquired by using the random sampling is reconstructed into the original waveform using spectrum-sparsity based reconstruction algorithms (to be developed). A key benefit is that the original waveform can be reconstructed from a relatively small number of signal samples. The major advantage of using the front-end THA (for random sampling) is that it provides a flexible setup for selection of sampling time-base signals (i.e. regular, pseudo-random, chirp, etc.) These time-base signals can be also switched on the fly by using programming digital control. The temporal combination of these time-base signals is optimized for data efficiency.

## 5.3 Publications

In the course of the dissertation research, the following journal articles, conference papers, and invention disclosures have been published.

### 5.3.1 Refereed Journal Articles

- H. Choi, A. Gomes, and A. Chatterjee, “Signal Acquisition of High-Speed Periodic Signals Using Incoherent Sub-Sampling and Back-End Signal Reconstruction Algorithms,” to appear in *IEEE Transactions on VLSI Systems*.
- H. Choi, D. Han, and A. Chatterjee, “Low-Speed Jitter Testing of High-Speed Digital Signals Using Time-Domain Jitter Expansion,” submitted to *IEEE Transactions on VLSI Systems*.
- H. Choi and A. Chatterjee, “Jitter Characterization of Incoherently Sub-Sampled Pseudo-Random Bit Sequences,” in preparation.

### 5.3.2 Conference Papers

- R. Senguttuvan, D. Han, H. Choi, S. Bhattacharya, and A. Chatterjee, “Adaptive OFDM Wireless Receiver Front-End: Self Correction and Self-Tuning,” 12th IEEE International Mixed-Signals Testing Workshop, June 2006.
- H. Choi, D. Han, and A. Chatterjee, “Enhanced Resolution Jitter Testing Using Jitter Expansion,” 25th IEEE VLSI Test Symposium, pp. 104–109, May 2007.
- R. Senguttuvan, H. Choi, D. Han, and A. Chatterjee, “A Novel Built-In Test Technique for Phase/Frequency Modulated RF Transmitters,” International GHz/Gbps Test Workshop 2007.
- H. Choi and A. Chatterjee, “Digital Bit Stream Jitter Testing Using Jitter Expansion,” IEEE Design, Automation and Test in Europe, pp. 1468–1473, Mar. 2008.

- R. Senguttuvan, H. Choi, D. Han, and A. Chatterjee, “Efficient Built-In Test of Phase/Frequency Modulated RF Transmitters Using Embedded Rectifier-Integrator Sensors,” 13th IEEE European Test Symposium, pp. 41–46, May 2008.
- V. Natarajan, H. Choi, D. Lee, R. Senguttuvan, and A. Chatterjee, “EVM Testing of Wireless OFDM Transceivers Using Intelligent Back-End Digital Signal Processing Algorithms,” IEEE International Test Conference, pp. 1–10, Oct. 2008.
- S. Kook, H. Choi, V. Natarajan and A. Chatterjee, “Low Cost Dynamic Test Methodology for  $\Sigma\Delta$  ADCs,” 18th Asian Test Symposium, pp. 69–74, Nov. 2009.
- H. Choi and A. Chatterjee, “Jitter Characterization of Incoherently Sub-Sampled High-Speed Digital Signals,” 16th IEEE International Mixed-Signals, Sensors, and Systems Test Workshop, June 2010.

### 5.3.3 Invention Disclosure

- H. Choi, D. Han, and A. Chatterjee, “Jitter Testing Technique Using Envelope Detection in Low-Speed Test Environment,” Provisional Patent Application 61/156,118, USPTO.

## APPENDIX A

### TIME-DOMAIN JITTER EXPANSION

In this appendix, jitter expansion is explained with detailed formulae. Notice that they follow the notations used in the previous sections.

Recall the models for a digital signal incorporating jitter and a reference signal described in Section 2.1 and Section 2.2.2

$$d(t) = A_d \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(t) \cdot e_i(t), \quad (43)$$

$$r(t) = A_r \cos\left(\frac{2\pi}{T_r} t\right), \quad (44)$$

respectively. The test case of  $\alpha = l$  is considered. Any sub-formulae in the two sections will be also used in this appendix without further explicit notes to reduce duplications.

First, a digital signal *without* jitter,  $\dot{d}(t)$ , is considered using the relation:  $t_i - t_{i-1} = T_d/2 \ \forall i$ .

$$\dot{d}(t) = A_d \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(t) \cdot \left(1 - e^{-\frac{t - i \cdot T_d/2}{\tau_d}}\right). \quad (45)$$

In addition, the relation below holds for a large  $n$  when  $\dot{d}(t)$  consists of bit patterns with the length of  $l$ .

$$\dot{d}(t) \approx \dot{d}(t - l \cdot T_d/2) \quad (46)$$

The two input signals  $\dot{d}(t)$  and  $r(t)$  are added together and result in  $\dot{s}(t)$ ,

$$\dot{s}(t) = \dot{d}(t) + r(t). \quad (47)$$

Assume that the envelope of  $\dot{s}(t)$  is determined by the amplitude maxima of  $\dot{s}(t)$  within every period of  $\dot{d}(t)$  (or  $l \cdot T_d/2$ ) and that one of the local maxima appears at

$t = \hat{t}$ , in other words,  $\dot{s}'(\hat{t}) = 0$ . That amplitude value is

$$\dot{s}(\hat{t}) = A_d \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(\hat{t}) \cdot \left(1 - e^{-\frac{\hat{t} - i \cdot T_d/2}{\tau_d}}\right) + A_r \cos\left(\frac{2\pi}{T_r} \hat{t}\right). \quad (48)$$

Then, consider a digital signal *with* jitter,  $\ddot{d}(t)$ , of the same bit pattern as what of  $\dot{d}(t)$ . Assume that the timing error value of the  $\ddot{d}(t)$  transition edge at which  $\hat{t}$  resides is  $\Delta$ . The summation of  $\ddot{d}(t)$  and  $r(t)$  is represented by

$$\ddot{s}(t) = \ddot{d}(t) + r(t). \quad (49)$$

Note that  $\ddot{s}(\hat{t}) \neq \dot{s}(\hat{t})$  because of the timing error,  $\Delta$ , injected to  $\ddot{s}(t)$ . To find the time at which  $\ddot{s}(t) = \dot{s}(t)$ ,  $\ddot{s}(t)$  is observed by *shifting* it a certain number of the  $\ddot{d}(t)$  period,  $\lambda \cdot l \cdot T_d/2$  (precisely,  $\Delta + \lambda \cdot l \cdot T_d/2$ ).

$$\begin{aligned} \ddot{s}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l) &= A_d \sum_{i=0}^{n+\gamma \cdot l} \alpha_i \cdot 1_{A_i}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l) \\ &\quad \cdot \left(1 - e^{-\frac{[\hat{t} + \Delta + \gamma(T_d/2)l] - [i \cdot T_d/2 + \Delta]}{\tau_d}}\right) \\ &\quad + A_r \cos\left(\frac{2\pi}{T_r}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l)\right). \end{aligned} \quad (50)$$

From the relation in Equation 46 and the assumption of very small  $\Delta$  (or  $\Delta \ll T_d$ ), the relation below is found

$$\begin{aligned} &\sum_{i=0}^{n+\gamma \cdot l} \alpha_i \cdot 1_{A_i}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l) \\ &\quad \cdot \left(1 - e^{-\frac{[\hat{t} + \Delta + \gamma(T_d/2)l] - [i \cdot T_d/2 + \Delta]}{\tau_d}}\right) \\ &= \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(\hat{t}) \cdot \left(1 - e^{-\frac{\hat{t} - i \cdot T_d/2}{\tau_d}}\right). \end{aligned} \quad (51)$$

Using the relation, Equation 50 can be simplified to

$$\begin{aligned} \ddot{s}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l) &= A_d \sum_{i=0}^n \alpha_i \cdot 1_{A_i}(\hat{t}) \cdot \left(1 - e^{-\frac{\hat{t} - i \cdot T_d/2}{\tau_d}}\right) \\ &\quad + A_r \cos\left(\frac{2\pi}{T_r}(\hat{t} + \Delta + \gamma \frac{T_d}{2} l)\right). \end{aligned} \quad (52)$$

The expanded jitter value is determined by the amount of additional *shift* that need be applied to  $\ddot{s}(t)$  for making the values of  $\dot{s}(t)$  and  $\ddot{s}(t)$  the same. Then, determining the expanded jitter value becomes solving Equation 52 for  $\gamma$ . For Equation 48 and Equation 52 to be the same value, the minimum value of  $\gamma$  should be chosen.

$$\Delta = -\gamma \cdot \left(\frac{T_d}{2}l - T_r\right) = \gamma \cdot T_{os}. \quad (53)$$

Finally, the jitter expansion ratio,  $\lambda$ , is derived as

$$\lambda = \left| \frac{\Delta + \gamma \frac{T_d}{2}l}{\Delta} \right| \approx \left| \frac{\gamma \frac{T_d}{2}l}{\Delta} \right| = l \cdot \frac{T_d}{2} / |T_{os}| \quad (54)$$

Note that  $\lambda$  for the test case of  $\beta = 1$  has not been explicitly derived for simplicity.

## APPENDIX B

### DISCRETE FREQUENCY AND TIME

A brief overview of discrete frequency and time is described in this appendix. The definitions of discrete frequency (in case of spectral aliasing) and discrete time are given as follows.

*Definition 1:* Discrete frequency  $f_d$ , as the analogue for discrete signals as analog frequency  $f_x$  is to continuous signals, is determined as

$$f_d = \frac{\min(|f_x - n \cdot f_s|)}{f_s} \cdot 2\pi, \quad (55)$$

where  $n$  is an integer, the function  $\min()$  returns the smallest value of the input arguments with various  $n$ ,  $f_s$  is the sampling frequency, and the discrete frequency value  $f_d$  is in the range of  $[0, \pi)$ . The function  $\min(|f_x - n \cdot f_s|)$  models spectral aliasing due to undersampling, and  $\frac{2\pi}{f_s}$  normalizes the discrete frequency to  $\pi$ .

*Definition 2:* Discrete time of a sampled signal is determined as

$$t_d[k] = \text{mod}(k \cdot f_d, 2\pi), \quad (56)$$

where  $k$  is the index of the sampled signal,  $f_d$  is the discrete frequency of the sampled signal, the function  $\text{mod}(x, y)$  returns  $(x - n \cdot y)$  and  $n$  is the greatest integer less than or equal to  $x/y$ , and the discrete time value  $t_d[\cdot]$  is in the range of  $[0, 2\pi)$ . Equation 56 is expanded and equivalent to Equation 24 shown in Section 3.1.2.2.

$$\begin{aligned} t_d[k] &= \text{mod}((k-1) \cdot f_d + f_d, 2\pi) \\ &= \text{mod}(\text{mod}((k-1) \cdot f_d, 2\pi) + f_d, 2\pi) \\ &= \text{mod}(t_d[k-1] + f_d, 2\pi). \end{aligned} \quad (57)$$

Note that the hat symbol attached to  $f_d$  in Equation 24 indicates an estimated value.

## APPENDIX C

### PROBLEMATIC SAMPLING COHERENCE

Incoherent sampling can be almost coherent even though not intended depending on the sampled signal frequency. Some of coherent sampling is problematic where multiple samples of a reconstructed waveform contain the same (or similar) discrete time value, which is called stuck samples in this paper. When such sampling coherency occurs and how to escape from the coherency are described in this appendix. First, coherent sampling is defined as follows.

*Definition 3:* Coherent sampling is the sampling of a periodic signal, where the sampled signal represents an integer number of its cycles within the sampled set.

$$\frac{f_d}{2\pi} = \frac{n_c}{n_s}, \quad (58)$$

where  $f_d$  denotes the (fundamental) discrete frequency of the sampled signal,  $n_c$  the integer number of cycles, and  $n_s$  the number of samples.

When the rational number  $n_c/n_s$  in Equation 58 is reducible, multiple samples of the sampled signal are stuck together in the reconstructed waveform in the discrete time domain  $[0, 2\pi)$ . As the result of such special cases of coherent sampling, gaps among samples in the discrete time domain may be too wide. Assuming that a gap larger than  $2/(2^\alpha\pi)$  is unacceptable, sampling at the following frequency bands is considered problematic in terms of sample distribution.

$$\frac{k}{2^{\alpha-1}\pi} - \Delta f_e < f_d < \frac{k}{2^{\alpha-1}\pi} + \Delta f_e, \quad (59)$$

$$\begin{aligned} \Delta f_e &= \left( \frac{2}{2^{\alpha-1}\pi} - \frac{2}{2^\alpha\pi} \right) / (n_s - 2^{\alpha-1}) \\ &= \frac{2}{2^\alpha(n_s - 2^{\alpha-1})\pi}, \end{aligned}$$



where  $f_d$  denotes the discrete frequency of the sampled signal,  $\Delta f_e$  the escape frequency,  $n_s$  the number of samples, and  $k = 0, 1, \dots, \alpha-1, \alpha$ . The equispaced frequency values  $k/(2^{\alpha-1}\pi)$  in Equation 59 correspond to the cases of stuck samples (the sampling coherence with the reducible rational number  $n_c/n_s$ ). By moving the sampling frequency apart from such frequency values, stuck samples start to separate. The escape frequency  $\Delta f_e$  is the amount of the frequency movement required to separate the samples and force the discrete time gaps less than or equal to  $2/(2^\alpha\pi)$ .

## APPENDIX D

### SUB-SAMPLING RATIO

The sub-sampling ratio  $R_s$  in the case a digital bit sequence of the bit width  $T_b$  is sampled at the rate of  $f_s$ , is defined by

$$R_s = \frac{1}{T_b \cdot f_s}. \quad (60)$$

If a clock signal of the bit width  $T_b$  is considered as a digital bit sequence to be sampled, the fundamental frequency of the clock signal is given by the value of  $1/(2T_b)$ .

In the case the clock signal is sub-sampled at the sub-sampling ratio of 1 (or at the sampling rate of  $1/T_b$ ), the fundamental tone of the clock signal is considered to be sampled at the Nyquist rate. The definition of the Nyquist rate  $f_N$  is given by

$$f_N = 2B, \quad (61)$$

where  $B$  is the highest frequency at which the signal can have nonzero energy.

## APPENDIX E

### DETERMINISTIC MODEL BASED POWER SPECTRAL DENSITY OF PHASE NOISE

In this appendix, the relation between the power spectral density (PSD) of a phase noise (or jitter) function, which describes how the power of a phase noise time series is distributed with frequency, and the PSD of a sinusoidal carrier signal that contains the phase noise is shown. To derive the relationship using closed-form formulae, a deterministic phase noise model is proposed. First, a phase-modulated carrier signal whose modulation function is a sinusoid is introduced. Later in this section, a chirp modulation function with time-varying amplitude is used to mimic the randomness of phase noise.

Modeling a phase modulated carrier signal  $y_c(t)$  yields

$$y_c(t) = A_c \cdot \cos(\omega_c t + \Delta\phi_m(t)), \quad (62)$$

$$\Delta\phi_m(t) = A_m \cdot \cos(\omega_m t),$$

where  $A_c$ ,  $\omega_c$ ,  $A_m$  and  $\omega_m$  denote the carrier signal amplitude, carrier signal angular frequency, modulation signal amplitude, and modulation signal angular frequency, respectively. The PSD (one-sided) of the phase modulation function  $\Delta\phi_m(t)$  is

$$S_{\Delta\phi_m}(\omega) = \frac{A_m^2}{2} \cdot \delta(\omega - \omega_m), \quad (63)$$

where  $\delta(\cdot)$  is the Dirac delta function. The carrier signal  $y_c(t)$  is rewritten as

$$y_c(t) = A_c \cdot \cos(\omega_c t + A_m \cdot \cos(\omega_m t)), \quad (64)$$

and expanded by applying trigonometric identities to

$$y_c(t) = A_c \cdot \cos(\omega_c t) \cdot \cos(A_m \cdot \cos(\omega_m t)) - A_c \cdot \sin(\omega_c t) \cdot \sin(A_m \cdot \cos(\omega_m t)). \quad (65)$$

This can be further expanded to yield

$$\begin{aligned}
y_c(t) = & J_0(A_m) \cdot A_c \cdot \cos(\omega_c t) \\
& + J_1(A_m) \cdot A_c \cdot \cos\left((\omega_c + \omega_m)t + \frac{\pi}{2}\right) + J_1(A_m) \cdot A_c \cdot \cos\left((\omega_c - \omega_m)t + \frac{\pi}{2}\right) \\
& + J_2(A_m) \cdot A_c \cdot \cos\left((\omega_c + 2\omega_m)t + \pi\right) + J_2(A_m) \cdot A_c \cdot \cos\left((\omega_c - 2\omega_m)t + \pi\right) \\
& + J_3(A_m) \cdot A_c \cdot \cos\left((\omega_c + 3\omega_m)t + \frac{3\pi}{2}\right) + J_3(A_m) \cdot A_c \cdot \cos\left((\omega_c - 3\omega_m)t + \frac{3\pi}{2}\right) \\
& + \dots,
\end{aligned} \tag{66}$$

where the function  $J_\alpha(x)$  is the Bessel function of the first kind. This indicates that an angle-deviation (phase modulation) gives rise to multiple sidebands (in the power spectrum) on each side of the carrier with a frequency spacing of  $f_m$  and an amplitude of  $J_\alpha(A_m) \cdot A_c$ . The PSD (one-sided) of the phase modulated signal  $y_c(t)$  is

$$\begin{aligned}
S_{y_c}(\omega) = & \underbrace{\frac{(J_0(A_m) \cdot A_c)^2}{2} \cdot \delta(\omega - \omega_c)}_{\text{carrier}} \\
& + \underbrace{\sum_{j=1}^{\infty} \frac{(J_j(A_m) \cdot A_c)^2}{2} [\delta(\omega - (\omega_c + \omega_m)) + \delta(\omega - (\omega_c - \omega_m))]}_{\text{side-bands}}.
\end{aligned} \tag{67}$$

In comparison with the one-tone phase modulation (from above), a linear chirp modulation tone with time-varying amplitude is used for deterministically modeling the phase noise (or jitter) of a carrier signal. The deterministic model of phase noise  $\Delta\phi_n(t)$  is given by

$$\Delta\phi_n(t) = \sum_{i=0}^{n-1} A_i \cdot \chi_{B_i}(t) \cdot \cos(2\pi\beta \cdot i \cdot t), \tag{68}$$

$$\begin{aligned}
\chi_{B_i}(t) &= \begin{cases} 1 & t \in B_i \\ 0 & t \notin B_i \end{cases}, \\
B_i &= [T \cdot i, T \cdot (i + 1)),
\end{aligned}$$

where  $A_i$  are the time-varying amplitudes of the modulation signal,  $B_i$  are time intervals,  $\chi_B$  is the indicator function of  $B$ , and  $\beta$  is the resolution bandwidth (RBW).

In this model, the value of  $\beta \cdot n$  is the phase noise bandwidth (of interest). The PSD (one-sided) of the phase noise function  $\Delta\phi_n(t)$  measured in the time interval of  $[0, T \cdot n)$ , is given by

$$S_{\Delta\phi_n}(\omega) = \sum_{i=0}^{n-1} \frac{A_i^2}{2n} \cdot \delta(\omega - \beta \cdot i), \quad (69)$$

under the assumption of  $T \gg 1/\beta$ . The carrier signal phase-modulated by the phase noise function  $\Delta\phi_n(t)$  is given by

$$y_{cn}(t) = A_c \cdot \cos(\omega_c t + \Delta\phi_n(t)) = A_c \cdot \cos\left(\omega_c t + \sum_{i=0}^{n-1} A_i \cdot \chi_{B_i}(t) \cdot \cos(2\pi\beta \cdot i \cdot t)\right), \quad (70)$$

and expanded to

$$\begin{aligned} y_{cn}(t) = & \chi_{B_0}(t) \cdot A_c \cdot \cos(\omega_c t + A_0) \\ & + \sum_{i=1}^{n-1} \chi_{B_i}(t) \cdot \left[ J_0(A_i) \cdot A_c \cdot \cos(\omega_c t) \right. \\ & + J_1(A_i) \cdot A_c \cdot \cos\left((\omega_c + \beta \cdot i)t + \frac{\pi}{2}\right) \\ & + J_1(A_i) \cdot A_c \cdot \cos\left((\omega_c - \beta \cdot i)t + \frac{\pi}{2}\right) \\ & + J_2(A_i) \cdot A_c \cdot \cos((\omega_c + 2\beta \cdot i)t + \pi) \\ & + J_2(A_i) \cdot A_c \cdot \cos((\omega_c - 2\beta \cdot i)t + \pi) \\ & + J_3(A_i) \cdot A_c \cdot \cos\left((\omega_c + 3\beta \cdot i)t + \frac{3\pi}{2}\right) \\ & + J_3(A_i) \cdot A_c \cdot \cos\left((\omega_c - 3\beta \cdot i)t + \frac{3\pi}{2}\right) \\ & \left. + \dots \right]. \end{aligned} \quad (71)$$

The PSD (one-sided) of the phase noise modulated carrier signal  $y_{cn}(t)$  measured in the time interval of  $[0, T \cdot n)$ , is given by

$$\begin{aligned} S_{y_{cn}} = & \underbrace{\left[ \frac{A_c^2}{2n} + \sum_{i=1}^{n-1} \frac{(J_0(A_i) \cdot A_c)^2}{2n} \right] \cdot \delta(\omega - \omega_c)}_{\text{carrier}} \\ & + \underbrace{\sum_{j=1}^{\infty} \sum_{i=1}^{n-1} \frac{(J_j(A_i) \cdot A_c)^2}{2n} [\delta(\omega - (\omega_c + \beta \cdot i)) + \delta(\omega - (\omega_c - \beta \cdot i))]}_{\text{side-bands}}. \end{aligned} \quad (72)$$

Consequently, the PSD (one-sided) of the phase noise function  $\Delta\phi_n(t)$  shown in Equation 69 can be converted to the PSD (one-sided) of the carrier signal with the phase modulation using the function  $\Delta\phi_n(t)$  as shown in Equation 72.

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## VITA

Hyun Choi was born in Seoul, Korea. He received the B.S. degree in electrical engineering from Korea University, Seoul, Korea, in 2004. He is currently a Ph.D. candidate in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta.

His research interests include high-speed digital/RF/mixed-signal measurement, test, diagnostics and physical characterization of advanced silicon and post silicon devices.